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SIGNAL CONDITIONING POWER PROGRAMMER

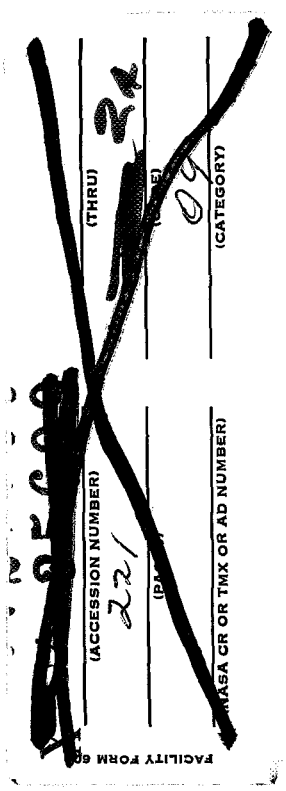
FINAL REPORT

REPORT NO. 05651-6001-R000 27 JAN 1967

Prepared for

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
MANNED SPACECRAFT CENTER
Houston, Texas

CONTRACT NO. NAS 9-5293



TRW SYSTEMS
AN OPERATING GROUP OF TRW INC.
ONE SPACE PARK REDONDO BEACH, CALIFORNIA

SIGNAL CONDITIONING POWER PROGRAMMER

FINAL REPORT

Report No: 05651-6001-R000

Prepared for

National Aeronautics and Space Administration
Manned Spacecraft Center
Houston, Texas

Contract No: NAS 9-5293

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FOREWORD

This work was performed by the Microelectronics Center of TRW Systems Group, TRW Inc., One Space Park, Redondo Beach, California, under National Aeronautics and Space Administration Contract Number NAS 9-5293, "Signal Conditioning Power Programmer." This report covers work conducted from 7 October 1965 through 7 December 1966 and is identified as Report Number 05183-6001-R000 by the Contractor. Members of the technical staff include David R. Breuer, Project and Design Engineer; Norman E. Grannis, Design Engineer, and James L. Buie, Section Head.

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1. INTRODUCTION

1.1 GENERAL DESCRIPTION

This report describes the work performed under contract NAS9-5293 to develop a microminiature 90-channel low-level signal conditioning system which features programmed power, conditioning of 5 millivolt full scale analog signals, and a IRIG specified PAM output. This system offers significantly reduced size, weight, and power combined with increased reliability over existing conventional low-level signal conditioning systems. A comparison is made in Table I.

TABLE I. COMPARISON OF CONVENTIONAL AND MICROMINIATURE 90-CHANNEL LOW-LEVEL SIGNAL CONDITIONING SYSTEMS

	Conventional	Microminiature	Reduction
Volume	750 in^3	< 50 in^3	<7%
Weight	45 lbs	< 2 lbs	<4%
Power	183 watts	5 watts	3%

Note: The microminiature volume and weight are estimates since system package design and fabrication were not included in this contract. The numbers refer to the complete system, including signal conditioners.

The following report includes the system, circuit, and device designs and the interdependency of each aspect. The system concept, for instance, is made practical by the development of the monolithic integrated circuit, low level dc amplifier under contract NAS9-3410. Adjustable evaporated cermet resistors on active silicon substrates, dielectric isolation, NPN-PNP transistors, MOSFET devices, MOS capacitors, and advanced circuit design techniques which incorporate these devices allow the system to be organized as described.

This contract includes the development and delivery of all circuits, except the signal modifiers, and includes a twelve-channel breadboard model which demonstrates the operation of the system.

1.2 SPECIFICATIONS

The contract specifications are found in Section 5, Test Procedures.

2. SYSTEM DESIGN

2.1 SYSTEM DESCRIPTION

The system concept is illustrated in the block diagram of Figure 1. The low level transducer outputs range from 5 to 100 millivolts full scale. A signal modifier converts the output of a transducer into a 0 to +5 volt full scale voltage. It may be dc amplifier, ac to dc converter, resistance to dc converter, or a phase sensitive demodulator, depending upon the type of sensor (see Appendix A).

Transducers, such as strain gauges, are sequentially energized via GTR gated voltage regulators. Power is likewise gated to signal modifiers, which are located on or near the transducers, via GMR gated voltage regulators. In the sequential mode of operation, all the channels are gated OFF, at any one time, except the channel being monitored. This gating technique allows the system power input to be significantly descreased.

Since the maximum system sequencing rate is limited by the thermal-electrical settling time of the signal modifiers, provision is also made to gate ON the modifier and/or transducer power one sample time in advance. This optional increase in the maximum sequencing rate is accomplished at the expense of increased power input. See Sections 2.2.2 and 2.4.

The outputs of the signal modifiers are multiplexed at a 0 to +5 volt full scale level and then conditioned into an IRIG specified PAM wave-train by the output circuit. The control logic, which operates in one of two modes, sequential or random access, provides control signals to the analog switches, power switches, and output circuit. The power source converts a +28 volt unregulated battery voltage into four regulated dc voltages. It includes a microminiature pulse width modulated power converter.

Some of the inherent advantages of the described microminiature signal conditioning system are:

a) Low level (5 millivolt full scale) inputs are conditioned;

b) Excitation power is supplied to transducers such as strain gauges;

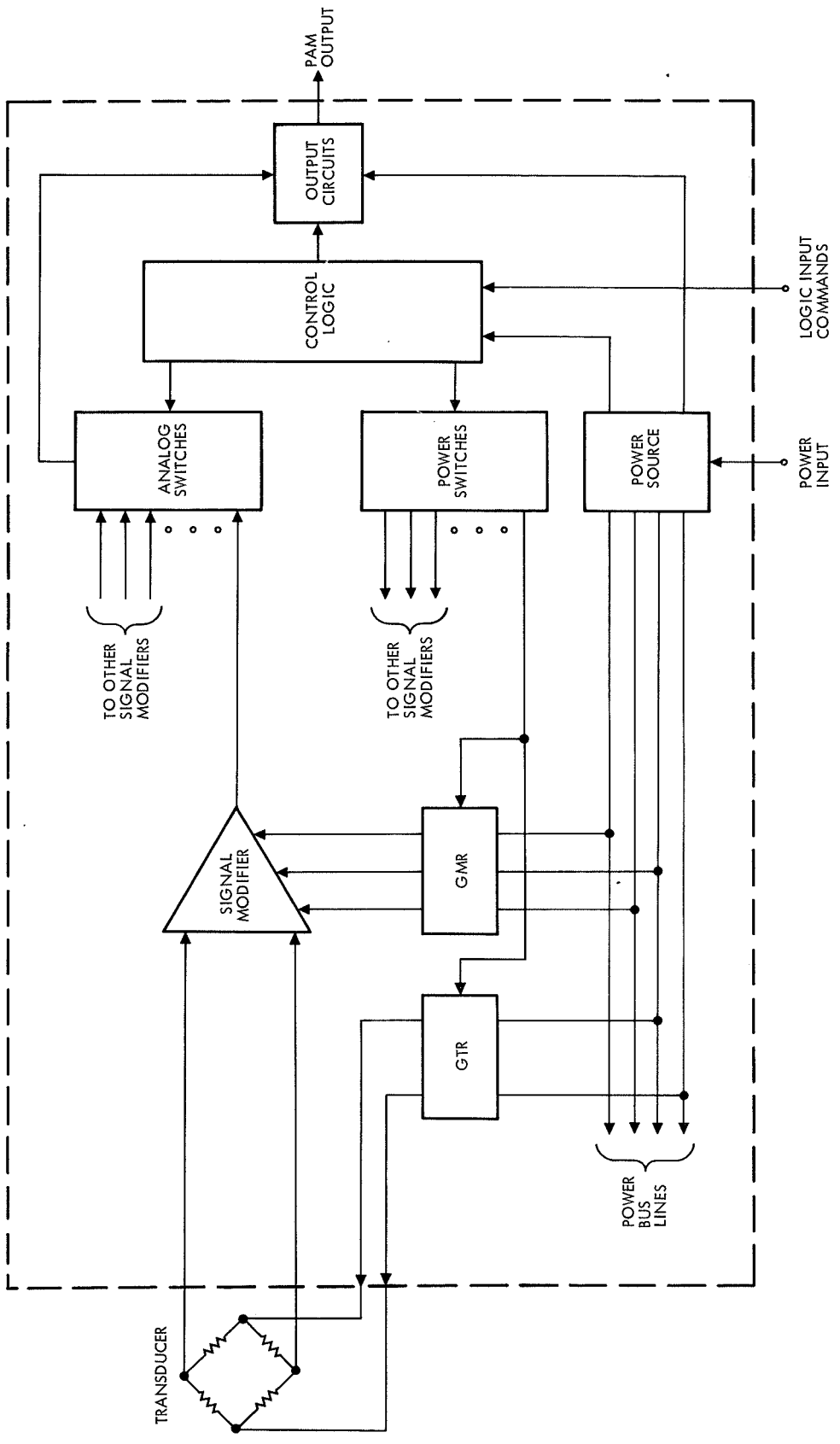


Figure 1. Signal Conditioning System Block Diagram

c) System power input is minimized by gating signal modifier and transducer power;

d) A signal modifier on each input channel provides flexibility in the type of analog signal to be conditioned;

e) A signal modifier on each analog input converts all signals to a high level before multiplexing, thereby minimizing analog errors normally encountered with long low level signal lines and low level multiplexers;

f) Crosstalk errors are minimized since all the channels are gated OFF, at any one time, except the channel being monitored;

g) The maximum speed of the system can be increased by turning ON each channel power in advance to the sample time.

See Appendix B for information on comparison with existing systems.

2.2 IDENTIFICATION AND SPECIFICATION OF BLOCK DIAGRAM FUNCTIONS

2.2.1 Transducers

A typical deflection bridge circuit is shown in Figure 2 in which a transducer such as a strain gauge, resistance thermometer, etc., forms one or more arms of the bridge. Variations in the transducer resistance(s) produce voltage variations which are amplified by the associated signal modifier. Bridge impedance levels of 350 ohms, or more, are excited by a ten volt precise voltage reference source. The bridge output signal levels under consideration range from 5 to 100 millivolts full scale. Strain gauge transducers have a susceptibility of shorts to the frame on which they are mounted, as shown in Figure 2. This short is anticipated in the design of the GTR voltage regulator to prevent the fault mode from being propogated into other channels of the system.

One output of the GTR is close to ground potential, +0.5 volt. The differential output voltage is 10 volts. Consequently, the common-mode input voltage to the signal modifiers is +5.5 volts.

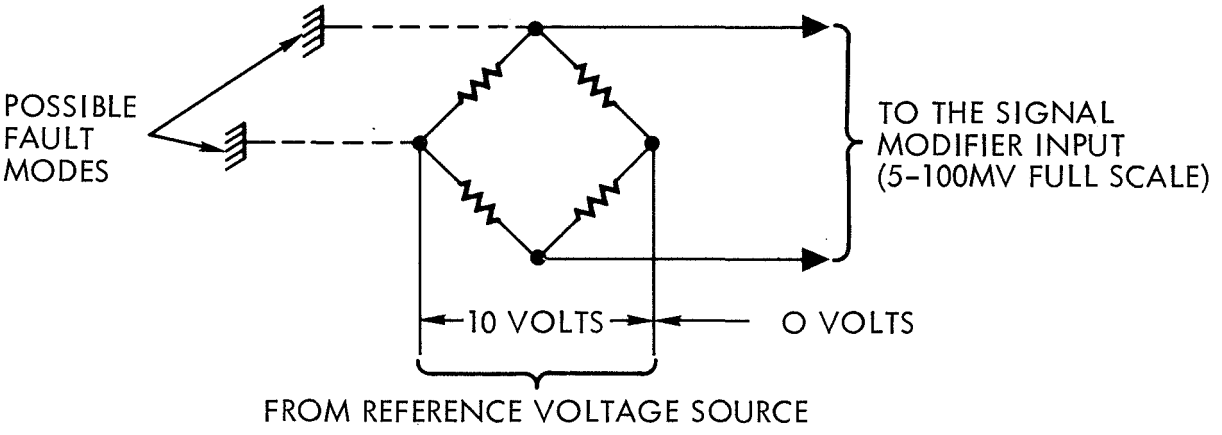


Figure 2. Typical Deflection Bridge Circuit

Note, the above discussion does not apply to channels monitoring transducers such as thermocouples, tachometers, flowmeters, voltage sources, etc., since no external excitation is required.

2.2.2 Signal Modifiers

The following information is included since it relates directly to the overall system performance and the specification of the remaining system blocks. The design, fabrication, and delivery of the signal modifiers are not included in this contract. However, the amplifier developed under contract NAS9-4640 is the basic building block of this family of signal modifiers. Table II indicates the pertinent specifications.

TABLE II. SIGNAL MODIFIER CHARACTERISTICS

Power supply voltages	+15 ±0.3 volt -15 ±0.3 volt
Power supply current	6 ± 1 ma
Output impedance	<1 ohm
Common-mode input voltage	<-1 volt to >+6.5 volts
Power switching settling time*	Case 1 150 μsec if differential 3 db Frequency response = 10 kHz Case 2 15 μsec if differential 3 db Frequency response > 100 kHz

*Settling times include gated regulator response time and assumes a 5 mv accuracy at the signal modifier output.

In Section 2.2.1 it was noted that the signal modifier common-mode input voltage is +5.5 volts for channels monitoring excited transducers. Therefore, assuming an additional ±1 volt for ac common-mode signals, the specification is set at -1 to +6.5 volts.

The amplifier delivered under contract NAS9-4640 requires capacitors to shape the 3 db frequency response at 10 kHz. These capacitors also limit the settling time to 150 μsec (Case 1). The settling time is the length of time needed for the amplifier to settle within 5 mv of its final value measured from the 50 percent point on the voltage regulator gate input signal. The settling time is reduced to 15 μsec by removing the differential roll-off capacitors (Case 2). This simultaneously increases the differential mode bandwidth and equivalent input noise.

See Appendix A for additional information on signal modifiers.

2.2.3 Gated Transducer Regulator (GTR)

The GTR provides a gated 10 volt reference voltage to transducers of 350 ohms or more. The block representation of Figure 3 shows the A/B power input, E/F power output, and C/D gate input signals. Transistor Q_A represents the series regulating element and transistor Q_B the saturating switch element.

Logic gate inputs V_C and V_D perform a logic OR function. When the gate signal V_C or V_D is high, Q_A is activated and Q_B is turned hard ON such that $(V_F - V_E)$ is regulated at 10 volts and V_E is the $V_{CE(SAT)}$ of Q_B. When the gate signal is low, Q_A and Q_B are turned OFF such that $(V_F - V_E) \simeq 0$ volts. The gate signal comes from the power switch matrix, which is equivalent to an open or closed switch to +5 volts. The OR capability of C/D inputs provides the option of turning ON the regulator one sample time in advance. T_{ON} is defined as the time required for the voltage output to settle within 5 mv of its final value, assuming the 50 percent point of the rising edge of the gate input signal as reference.

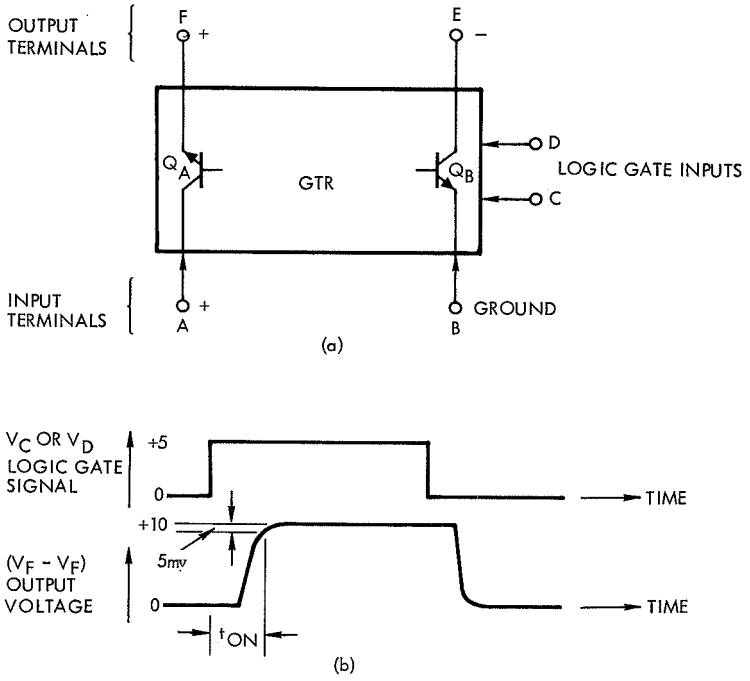


Figure 3. Gated Transducer Regulator

Both the positive and negative lines are disconnected during OFF to prevent a shorted transducer from affecting other channels via ground loops. The regulator is short circuit protected to limit the power supply current if a transducer is shorted.

The current drawn by the GTR during OFF is limited to semiconductor leakage currents so that the OFF power dissipation is minimum. This feature minimizes the system power consumption. Table III lists the important specifications of the GTR.

TABLE III. GTR SPECIFICATIONS

	ON			OFF		
	Minimum	Typical	Maximum	Minimum	Typical	Maximum
V_A (volt)	+15	+16	+18	+15	+16	+18
V_B (volt)		0			0	
V_C or V_D (volt)		+4.7			0	
V_E (volt)		0.3	0.5		0	0.01
$V_F - V_E$ (volt)	9.950	10.000	10.050		0	0.01
I_L (ma)	30		60		0	0.01
I_S (ma)		$2I_L$				
P_D (mw)		215			0	0.18
T_{ON} (μsec)			20			
Temp (^oC)	-35	+25	+95	-35	+25	+95

where

$I_L \equiv$ Load current

$I_S \equiv$ Short circuit current

$P_D \equiv$ Power dissipation

$(V_F - V_E)$ minimum and maximum include effects of temperature, line and load variations

2.2.4 Gated Modifier Regulator (GMR)

The GMR provides a gated 30 volt supply to the signal modifiers, which draw 6 ±1 ma during ON. The block representation of Figure 4 shows the A/B/C power inputs, F/G power outputs, and D/E gate inputs. Transistor Q_A represents the series regulating element and transistor Q_B the saturating switch element.

Logic gate inputs V_D and V_E perform a logic OR function. When the gate signal V_D or V_E is high, Q_A is activated and Q_B is turned hard ON, such that $(V_G - V_F)$ is regulated at 30 volts and V_F is approximately -15 volts or $V_C - V_{CE(sat)Q_B}$. When the gate signal is low, Q_A and Q_B are turned OFF, such that V_F and V_G go to ground potential. This is necessary to insure that the signal modifier draws negligible current during OFF. The gate signal comes from the power switch matrix which is equivalent to an open or closed switch to +5 volts. The OR capability of D/E inputs provide the option of turning ON the regulator one sample time in advance. T_{ON} is defined as the time required for the voltage output to settle within 100 mv of its final value, assuming the 50% point of the rising edge of the gate signal as reference.

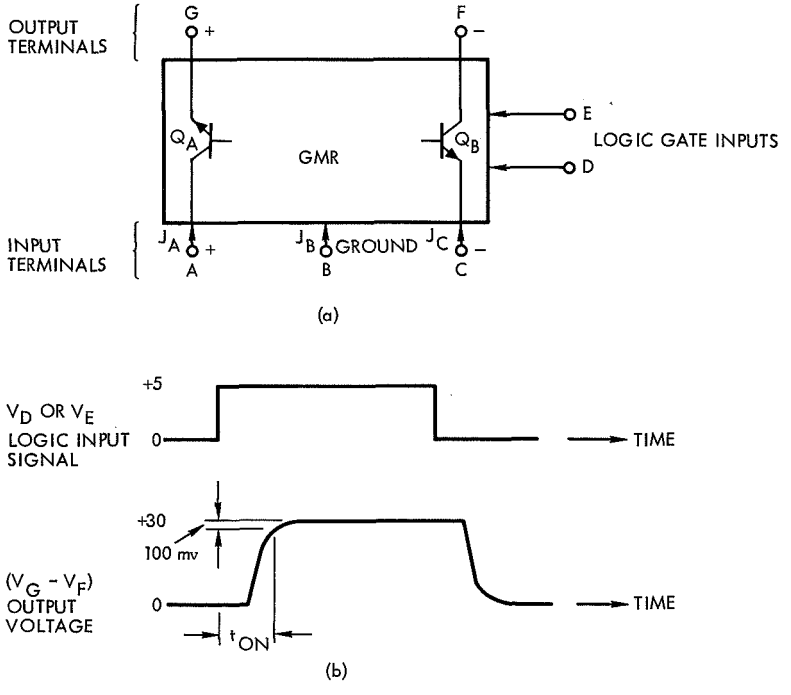


Figure 4. Gated Modifier Regulator

Both the positive and negative lines are disconnected during OFF to minimize the signal modifier OFF currents. This feature minimizes the system power consumption. Table IV lists the important specifications of the GMR.

TABLE IV. GMR SPECIFICATIONS

	ON			OFF		
	Minimum	Typical	Maximum	Minimum	Typical	Maximum
V_A (volt)	+21	+23	+25	+21	+23	+25
V_B (volt)		0			0	
V_C (volt)	-14.6	-15.1	-15.6	-14.6	-15.1	-15.1
V_D or V_E (volt)		+4.7			0	
V_F (volt)		-15			0	0.01
(V_F-V_G) (volt)	29.7	30.0	30.3		0	0.01
I_L (ma)	5	6	7		0	0.01
I_A (ma)		8.2				
I_B (ma)		0.45				
I_C (ma)		7.75				
P_D (mw)		125			0	0.3
T_{ON} (μsec)			20			
Temp (^oC)	-35	+25	+95	-35	+25	+95

where

$I_L \equiv$ Load current of positive line

$P_D \equiv$ Power dissipation

(V_F-V_G) minimum and maximum include effects of temperature, line and load variations

2.2.5 Power Switch Matrix

The power switch matrix shown in Figure 5 is a serial-to-parallel converter which distributes +5 volts through a series impedance to 88 outputs, one at a time. It functions as a single pole, eighty-eight position switch. The 88 outputs are used as gating signals for the GTR and GMR gated regulators.

The power switch matrix is divided into a three level AND function and is controlled by a three digit octal code received from the control logic block. Each output of the power switch matrix measures either an open circuit (>100 megohms) or a low impedance (<2K ohms) to +5 volts. When a power switch matrix output is connected to +5 volts, the regulator which is connected to that output is turned ON. Only one output is connected to +5 volts at any one time for both the sequential and the parallel modes of operation. The timing diagram of Figure 6 shows the outputs in the sequential mode of operation.

2.2.6 Analog Switch Matrix

The analog switch matrix shown in Figure 7 is a parallel-to-serial converter which connects the input of the PAM circuit to the outputs of the 88 signal modifiers, one at a time. It functions as a single pole, eighty-eight position commutator. The analog switch matrix is divided into a three-level AND function and is controlled by the same three-digit octal code which controls the power switch matrix. Only one signal modifier is connected to the PAM circuit at any one time, for both the sequential and the parallel modes of operation. Figure 8 shows the timing diagram for the sequential mode of operation. The analog switch matrix introduces less than 0.1 percent error in the analog signal being conditioned.

2.2.7 Control Logic

The control logic block shown in Figure 9 provides digital control signals for the power switch matrix, analog switch matrix and PAM output circuit. Modes of operation include sequential or random access

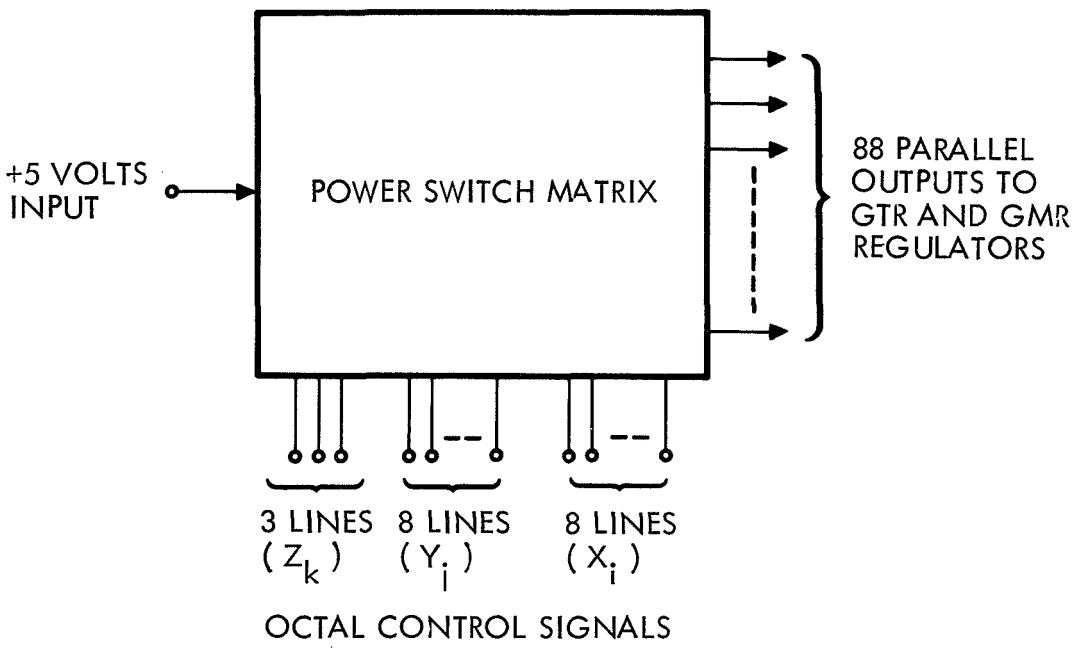


Figure 5. Power Switch Matrix Block Diagram

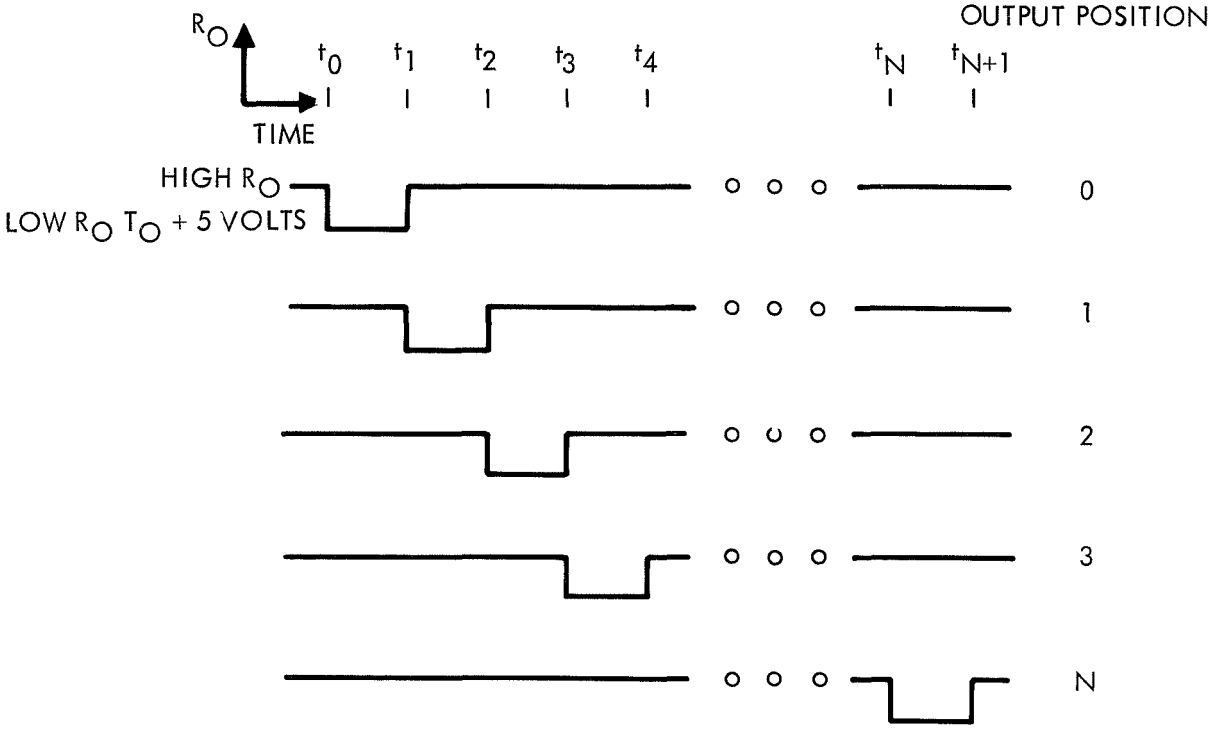


Figure 6. Power Switch Timing Diagram for Switching Mode

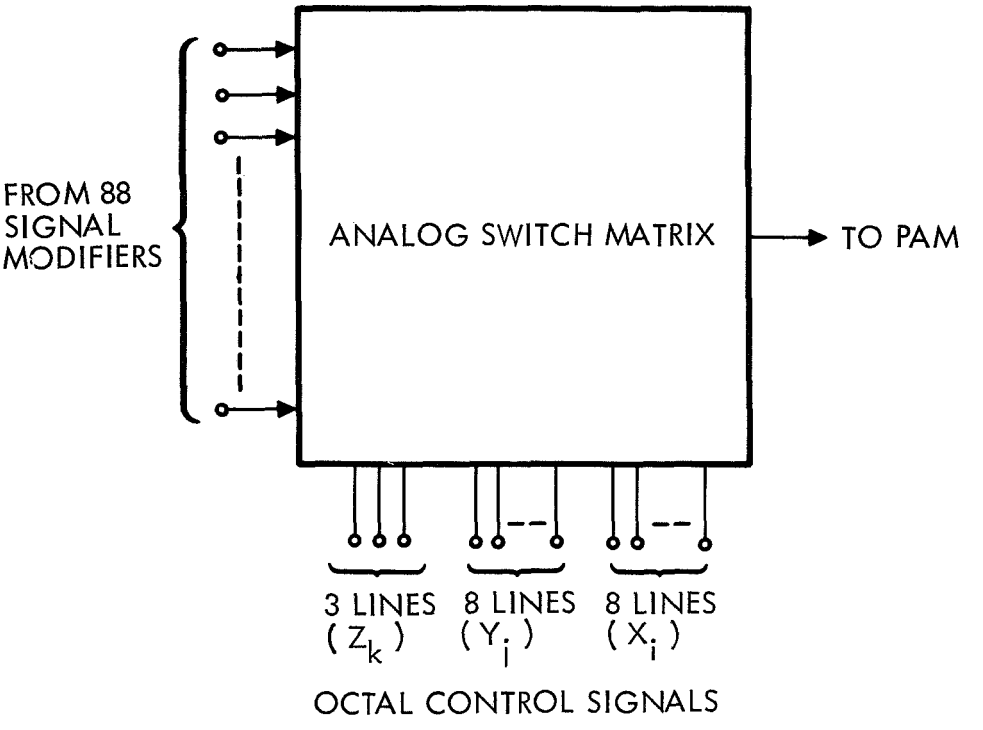


Figure 7. Analog Switch Matrix Block Diagram

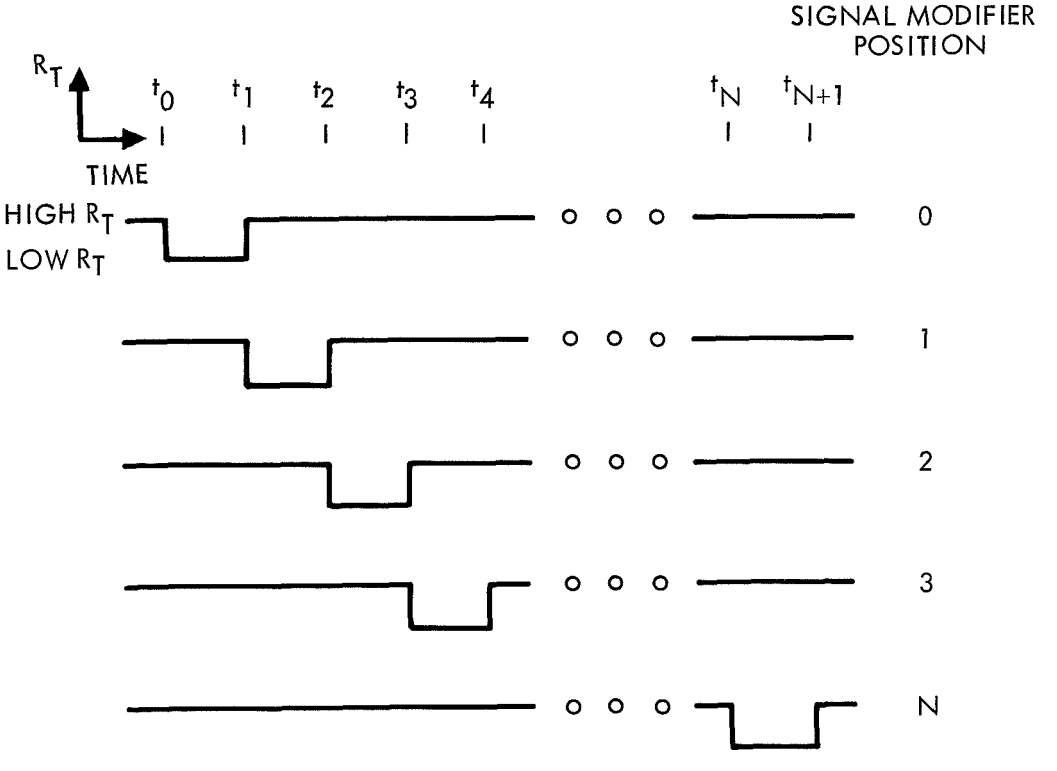


Figure 8. Analog Switch Matrix Timing Diagram for Switching Mode

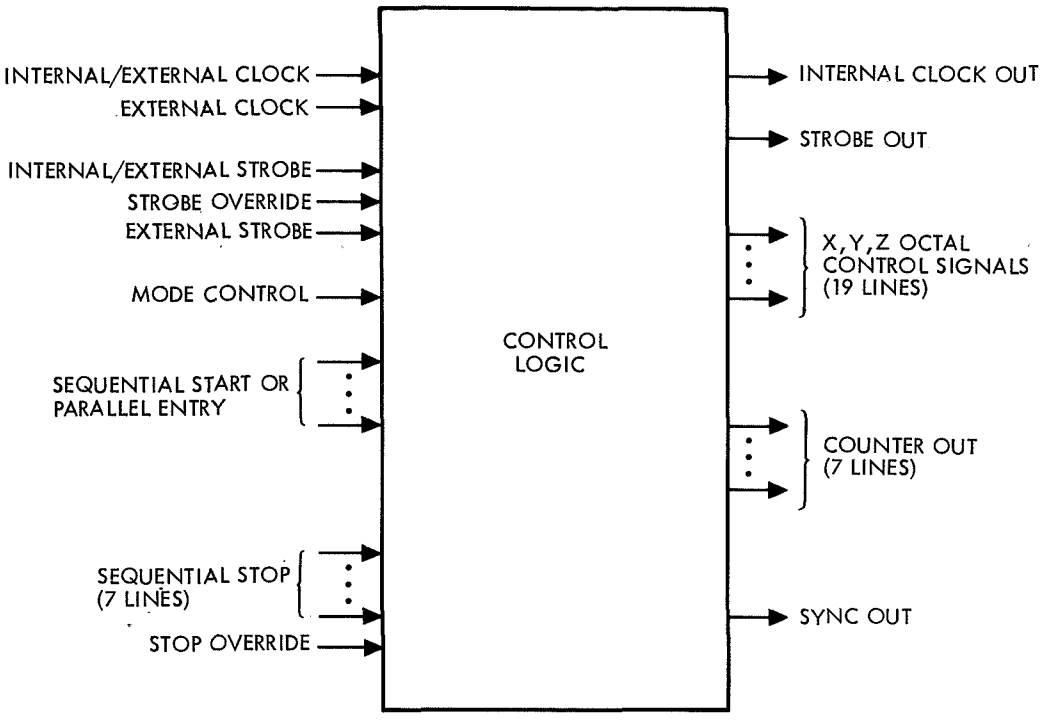


Figure 9. Control Logic Input/Output Signals Block Diagram

channel selection, and internal or external control. If all the logic inputs are disconnected, the programmer will automatically sequence through all the channels at the specified sampling rate of 900 Hz. All logic input signals are of the type that require an equivalent of a switch closure to ground for the active level and an open line or positive voltage for the normal level. All digital signals entering or leaving the programmer are short circuit proof and may be shorted either to ground or to each other without damaging the programmer.

The description of the control logic input/output signals are as follows:

a) INPUTS

NOTE: Unless specified otherwise, the following specifications apply to all digital inputs:

Logic 0 level: 0 ± 0.5 volts
Logic 0 load: 150 μA maximum to 5.5 volts maximum

Logic 1 level: Disconnected or at 5 ±2 volts
Logic 1 load: 5 μA maximum to GND

INT/EXT CLOCK	Logic level used to select between an internal or external source for the clock signal which determines the basic channel scan rate. Logic 1 selects the 900 Hz internal clock; logic 0 selects the signal connected to the EXT CLK input. Logic 1 load: 10 μA maximum to GND; logic 0 load: 300 μA maximum to 5.5 volts.
EXT CLOCK	When selected by the INT/EXT CLK line, this input provides the clock signal which determines the basic channel scan rate. Programmer steps to next channel on transition from logic 1 to logic 0. Minimum pulse duration at logic 1 level: 400 ns. Frequency range: dc to 100 kHz.
INT/EXT STROBE	Logic level used to select between an internal or external source for the strobe signal used to sample the analog voltage. Logic 1 selects the internal strobe derived from the clock signal; logic 0 selects the signal connected to the EXT STROBE input. Logic 1 load; 10 μA maximum to GND; logic 0 load: 300 μA maximum to 5.5 volts.
$\overline{\text{STROBE OVR}}$	Overrides strobe inputs by providing a continuous active level for the STROBE signal. Logic 0 is override condition, logic 1 has no effect on programmer.
EXT STROBE	When selected by the INT/EXT STROBE line, this input provides the strobe signal used to sample the analog output voltage. Sampling will occur when the signal is at the logic 1 level. Minimum pulse duration at logic 1 level: 400 ns. Frequency range: dc to 100 kHz.

MODE CONTROL	Inhibits scanning when at the logic 0 level. No effect on programmer when at logic 1. Logic 1 load: 10 μA maximum to GND; logic 0 load: 260 μA maximum to 5.5 volts maximum.
SEQUENTIAL START or PARALLEL ENTRY	Seven-bit binary input data. During parallel mode operation, the programmer monitors the channel corresponding to the code set up by these 7 lines, but only when the $\overline{\text{PAR LOAD}}$ signal is activated. In serial mode operation, the start channel corresponds to the code set up by these inputs. Logic 1 level = binary 0, logic 0 level = binary 1 (false inputs).
$\overline{\text{PARALLEL LOAD}}$	In parallel mode operation, this signal is used in conjunction with binary input data $\overline{\text{b1-b64}}$. Signal is normally at logic 1 and pulsed to logic 0. Binary inputs will not effect programm unless $\overline{\text{PAR LOAD}}$ is at logic 0 level. Minimum pulse duration at logic 0 level: 400 ns. Frequency range: dc to 100 kHz. Binary inputs must be static during pulse interval. Logic 1 load: 5μA maximum to GND; logic 0 load: 1.6 μA maximum to 5.5 volts maximum.
SEQUENTIAL STOP	Seven-bit binary stop code. In serial mode operation, the programmer stops on the first channel after the channel corresponding to the code determined by the state of these lines. Since the programmer automatically restarts itself, this code corresponds to channel N-1, where N is the last channel in a continuously repeating cycle. Logic 1 level = binary 1, logic 0 level = binary 0 (true inputs).

STOP OVERRIDE	Overrides stop code selected by S1-S64. Logic 0 causes programmer to cycle from start channel all the way through to last channel (channel 127). Logic 1 has no effect on programmer.

b) OUTPUTS

NOTE: Unless specified otherwise, the following specifications apply to all digital outputs:

Logic 0 level: 0V minimum to +0.45 volt maximum
Logic 0 load: 10 mA maximum to +7V maximum
Logic 1 level: 2.5 V minimum 5.5 V maximum
Logic 1 load: 100 μA maximum to GND
Logic 1 to logic 0 transition (90 to 10%): 500 ns maximum with 100 pF to GND
Logic 0 to logic 1 transition (10 to 90%): 2 μs maximum with 100 pF to GND

INT CLOCK OUT	Continuous 900 Hz 50 percent duty cycle square wave. Can be used for synchronization purposes or for test signal. When programmer scan rate is controlled by internal clock, programmer steps from one channel to next on logic 1 to logic 0 transition of this signal. If PAM is used, analog data is sampled during positive half of INT CLK OUT waveform.
STROBE	Controls analog data sample period in PAM output circuit. When strobe is logic 1, PAM circuit samples analog signal. When strobe is logic 0, PAM circuit is 0 volts.
X, Y, Z OCTAL CONTROL SIGNALS	Three digit octal code which controls power and analog switch matrices. Unique channel position, 0 through 127, designated by this code. Logic levels shifted to be compatible with switch matrices requirements. Logic 1 = +5 ±2 volts. Logic 0 = -15 ±1.5 volts.

COUNTER BINARY OUT	Seven-bit binary code which indicates present channel position. Normally connected as required to stop inputs (S1-S64), these seven lines may be connected also to an external display, etc., which can then monitor the position of the programmer. Logic 1 = binary 1, logic 0 = binary 0 (true outputs).
SYNC OUT	Used to synchronize PAM output to external test equipment. This signal is a positive pulse occurring during the last half of channel N-1 and both halves of channel N, where N is the last channel before restarting. Positive level = logic 1, normal level = logic 0.

2.2.8 PAM Output Circuit

The PAM output circuit converts the output of the analog switch matrix into an IRIG specified PAM wavetrain. Typical input/output waveforms, together with the block diagram, are shown in Figure 10.

V_1 is the multiplexed analog signal from the output of the analog switch matrix. Figure 10(b) shows an example waveform in which channels 0 and 1 are full scale and zero, respectively, and channels 82 through 87 are an increasing staircase with one volt pedestals. The PAM output circuit samples this waveform during the last 50 percent of the channel period as ON period; however, the difference is only academic. The waveforms are identical. This circuit performs an algebraic manipulation on the analog signal according to the equations:

$$V_3 = 0.8V_1 + 1.0 \quad \text{(ON period)} \tag{1}$$

$$V_3 = 0 \quad \text{(OFF period)} \tag{2}$$

such that a zero level analog signal is presented as a 1 volt output and a full-scale, 5 volt level is presented as a 5 volt output. The strobe signal from the control logic section is shown as V_2 in Figure 10(c). When this

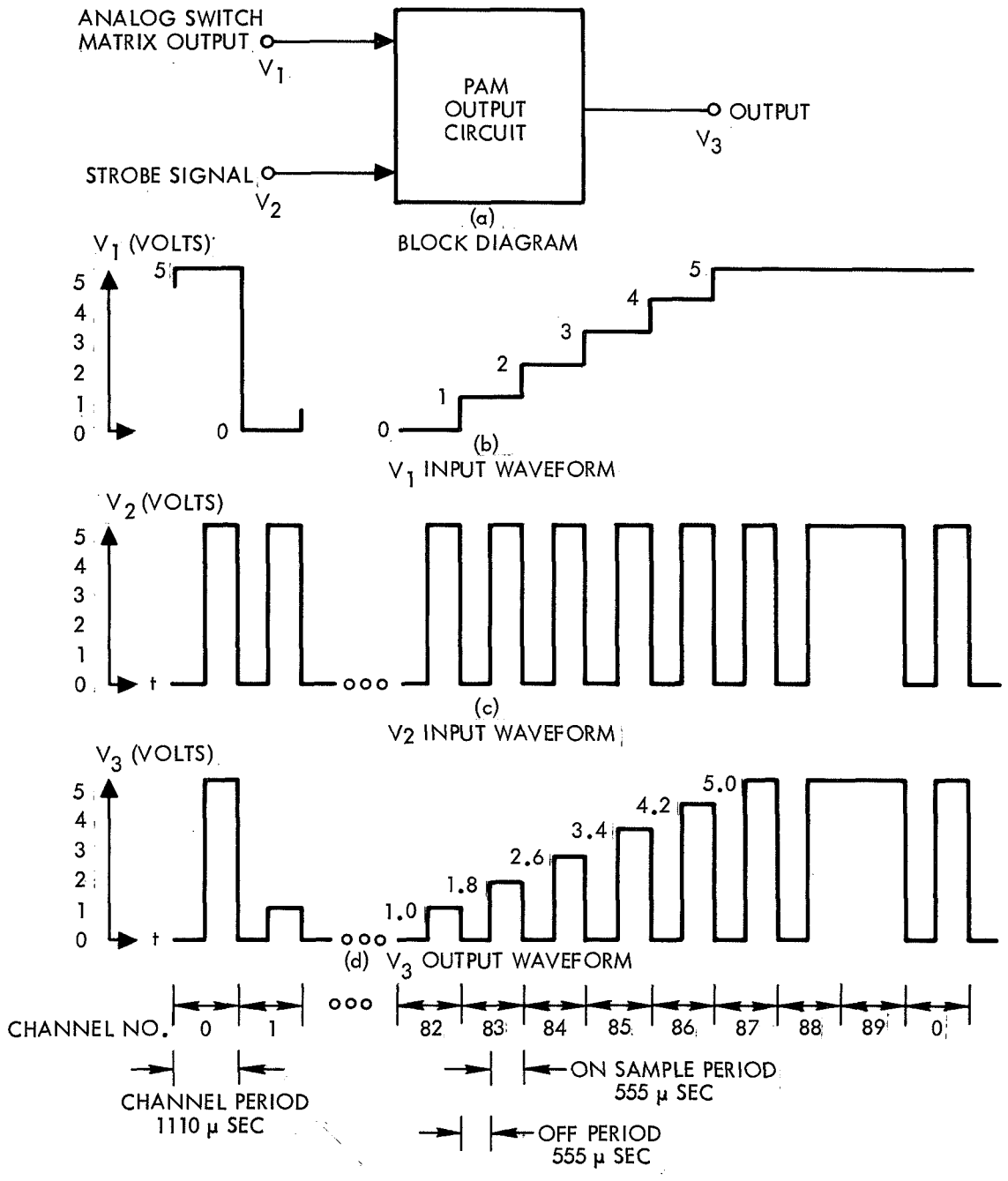


Figure 10. PAM Output Circuit Block Diagram and Input/Output Waveforms

signal is at logic 1 level, Equation (1) applies. When V_2 is at logic 0 level, Equation (2) applies. The resultant output is shown as V_3 in Figure 10(d).

The last two channels, shown as channels 88 and 89, are reserved for PAM wavetrain synchronization or frame identification. The IRIG specifications require that the last 50% of the next to the last channel, 88, and all of the last channel, 89, be held at +5 volt, as shown in Figure 10(d).

The PAM output circuit specifications are as follows.

2.2.8.1 Synchronization

The PAM synchronization pulse shall be internally generated with an amplitude of 5 volts ±1 percent and shall occur during the ON time of the (N-1) channel and during the ON and OFF time of the (N) channel, where N denotes the last programmed channel.

2.2.8.2 Duty Cycle

The PAM duty cycle shall be 50 ±3 percent where

$$\text{Duty Cycle} \equiv \frac{\text{ON Sample Period}}{\text{Channel Period}}$$

2.2.8.3 Channel Period

The PAM channel period shall be 1110 ±50 μsec. For a full 90-channel system, the frame rate is 10 frames per second.

2.2.8.4 Zero Data Pedestal

With a channel input of zero volts, the PAM pulse amplitude shall be 1 ±0.050 volt.

2.2.8.5 Full Scale Output Amplitude

For a full scale amplifier output voltage of +5.000 volts, the PAM pulse amplitude shall be +5 ±0.050 volt.

2.2.8.6 Pulse Amplitude Stability

The amplitude of any PAM channel output pulse shall remain constant within ±1 percent of full scale under all electrical and environmental conditions specified.

2.2.8.7 OFF Time Voltage

The level of the PAM output between sample periods shall be zero ±0.050 volt.

2.2.9 Power Source

The power source converts the 28 volt unregulated battery voltage into five regulated voltages; V_1 to provide a precise reference voltage, V_2 to power the gated transducer regulators, V_3 and V_4 to power the gated modifier regulators, and V_5 to power the control logic. Figure 11 shows the block configuration.

A microminiature power converter provides electrical isolation (transformer coupling) and pre-regulation. This direct compensation, pulsewidth modulation converter operates at 200 kHz switching rate. No overall feedback loop is used. The four converter outputs are further conditioned by the RR, TPR16, MPR38, MPR16, and LR series regulators to insure excellent line regulation and ripple rejection. If overall feedback is included in the converter (as proposed future models will), these series regulators will not be required, except for the RR reference regulator, thereby increasing the efficiency of the power source. Table V gives the input-output specifications of the power source.

a) Input. The power source shall be powered from an external battery. The characteristics of this battery are as follows:

- The voltage is between 22 and 32 volts with 28 volts being nominal.
- There is a possible maximum 4 volt peak-to-peak ripple (dc to 2 kc square wave) impressed upon the battery voltage. The battery voltage, including the ripple, will be between 22 and 32 volts.

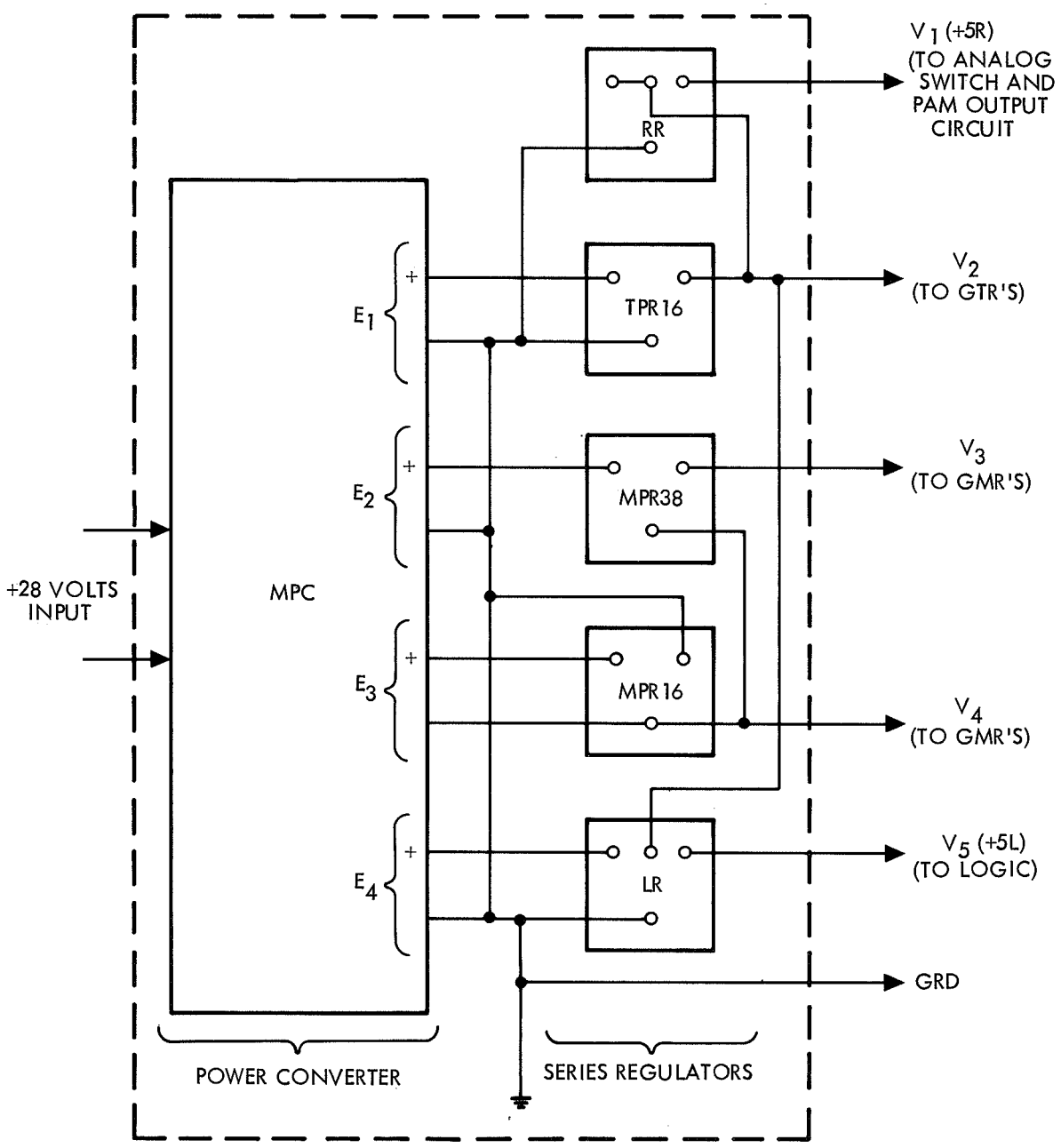


Figure 11. Power Source Block Diagram

- There is a possible transient on the power line that may reduce the battery voltage to as low as 0 volts or increase it to as high as 43 volts. This transient has a 20 millisecond basewidth duration and an 8 millisecond rise time.

- The circuitry connected to the battery is required to survive this transient, but the specification performance is not required. Operation shall return to normal within 100 microseconds after the duration of the pulse.

b. Outputs

TABLE V. POWER SOURCE INPUT/OUTPUT SPECIFICATIONS

	Voltage			Output Voltage	Current Drawn		
	Minimum	Typical	Maximum	Stability	Minimum	Typical	Maximum
V_1	4.980	5.000	5.020	0.4%		100 ua	
V_2	15.5	13.0	16.5	3%	33 ma		67 ma
V_3-V_4	37.0	38.0	39.0	5%	18 ma		26 ma
V V_4	15.35	15.5	15.65	1%	18 ma		26 ma
V_5	4.8	5.0	5.2	4%	40 ma		60 ma

The min-typ-max output voltage specifications include effects due to line, load, and temperature variations in addition to initial setting. The maximum current drawn from the V_2, V_3, and V_4 terminals is determined by the switching mode selected for the gated regulators. For instance, minimum current is drawn if neither the GTR or GMR are turned on in advance of the channel period. Maximum current is drawn if both the GTR and GMR are turned on in advance (see Section 2.4).

2.3 CONTROL LOGIC DESIGN

The major subsections of the control logic as shown in Figure 12, are:

a) Internal multivibrator and clock select logic

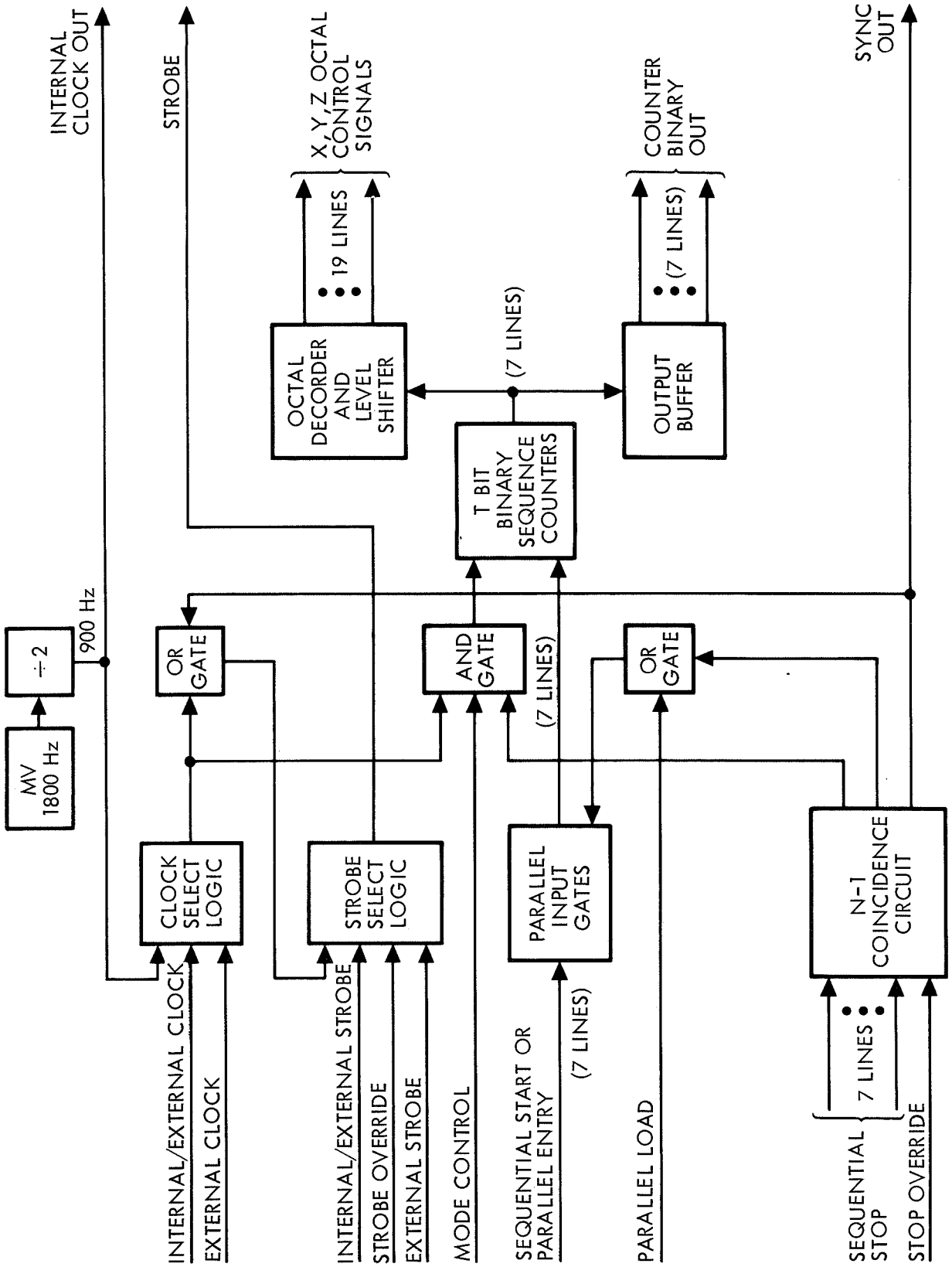


Figure 12. Control Logic Subsection Block Diagram

b) Seven-bit binary sequence counter

c) Octal decoder and level shifter

d) Parallel input control

e) Sequential start-stop control (includes output buffers, N-1 coincidence circuit, and parallel input gates)

f) Strobe circuit.

Particular attention has been given to the choice of logic elements or basic building blocks. Low-power diode-transistor logic (DTL) in the form of NAND gates is used throughout the control logic (1 mw per gate, 4 mw per flip-flop). This provides high noise immunity as well as excellent speed characteristics. Section 3.4 gives the circuits.

The master-slave technique is employed with the flip-flops so that all logic throughout the system is directly coupled and does not require specific rise and fall times. Since no ac coupled inputs are used, the operation of the logic depends only upon voltage levels. Therefore, the system behavior is relatively independent of waveshape, requiring only that the proper voltage levels be maintained. All outputs employ buffer amplifiers to increase their drive capability and to isolate externally generated noise from internal logic. All inputs are short circuit proof. A brief description of each section follows.

2.3.1 Internal Multivibrator and Clock Select Logic

The internal multivibrator clock oscillates at 1800 Hz 3 percent and drives a divide-by-two flip-flop, as shown in Figure 13, to develop a 900 Hz clock signal. The resultant channel period in the automatic sequential mode is 1110 sec and the programmer frame rate is 10 frames per second. Buffer amplifiers isolate the flip-flop output from the INT CLK OUT. An INT/EXT CLK signal selects the internal or an external clock. Switching rates up through 100 kHz can be used via the external clock input.

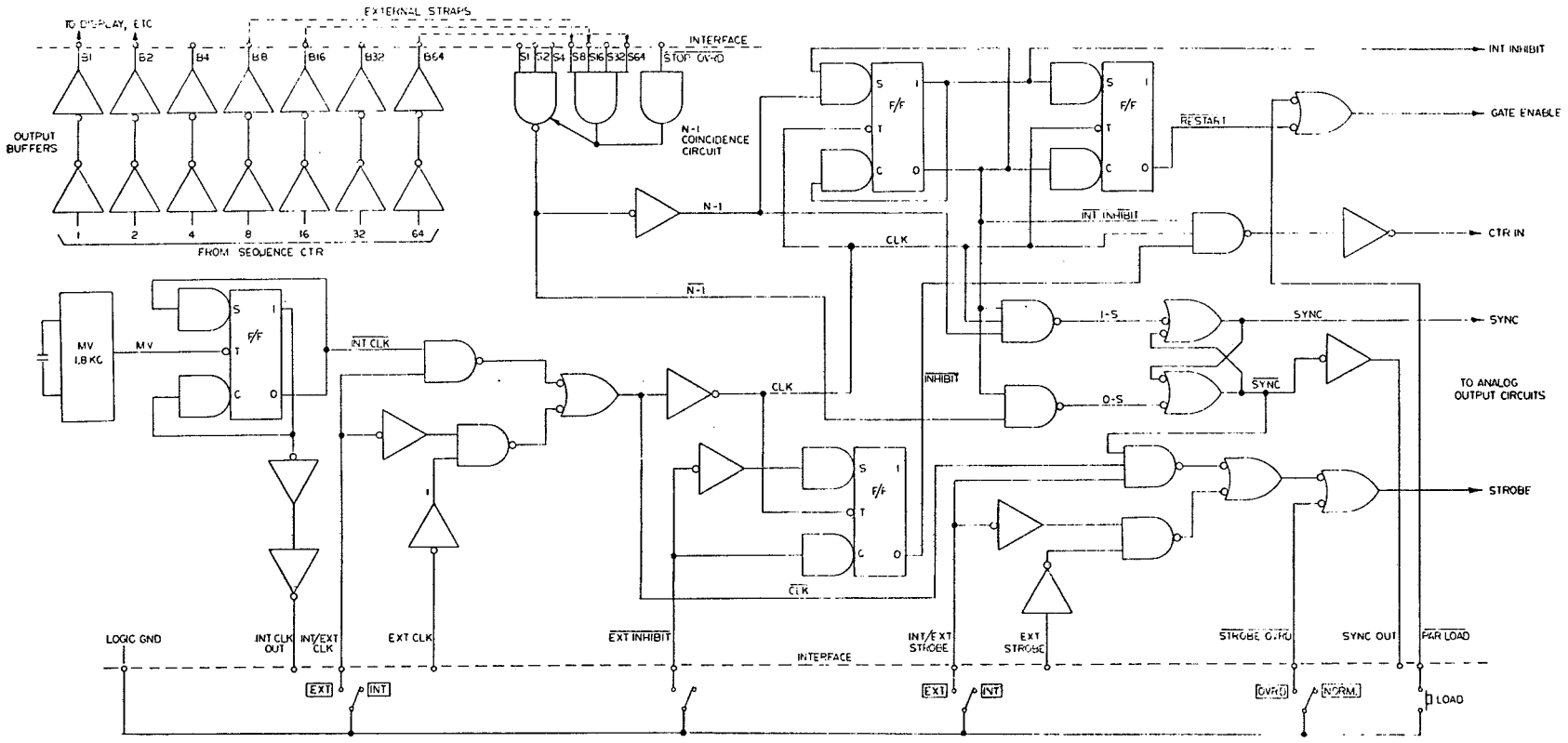


Figure 13. General Logic for Control and Clock

Although it is not required by the sequence counter, the CLK output is used elsewhere by the strobe circuit, and thus the multivibrator output is chosen twice frequency and divided by two in order to obtain the precise 50 percent duty cycle CLK line required by the strobe circuit. By selecting the external clock, a means for synchronizing the scan rate of the programmer to external equipment is afforded.

2.3.2 Seven-Bit Binary Sequence Counter

The heart of the control logic is the sequence counter, shown in Figure 14. Its function is to generate coded outputs used by the decoder and output buffers to determine which channel has been selected for connection to the output circuits. As a synchronous serial-carry binary counter, it uses sever dc flip-flops to generate 14 binary coded lines (7 true, 7 false) which are fed to the decoder and output buffers. Use of a synchronous carry (clocked) technique, rather than a ripple carry, effectively eliminates the unwanted decoding spikes caused by the delays inherent with a ripple carry counter. The counter may be advanced serially one bit at a time (and, consequently, one channel at a time) by trigger pulses occurring on the CTR INPUT line, or alternatively, it may be jam-set to any binary code by energizing the appropriate outputs of the parallel input gates. The only restriction to controlling the counter is that the serial and parallel inputs do not occur at the same time. Note that with seven bits the counter can assume up to 128 unique states, thus corresponding to a maximum of 128 channels.

2.3.3 Octal Decoder and Level Shifter

The outputs of the counter are connected to the octal decoder, as described in the previous paragraph and shown in Figure 15. The decoder takes the first three least significant bits and converts them into an octal number between 0 and 7. At the same time, it level shifts the signals to voltage levels that are compatible with the MOSFET switch matrices. These eight output lines are designated X0 through X7. Similarly, the next three bits are converted to eight lines designated YO through Y7,

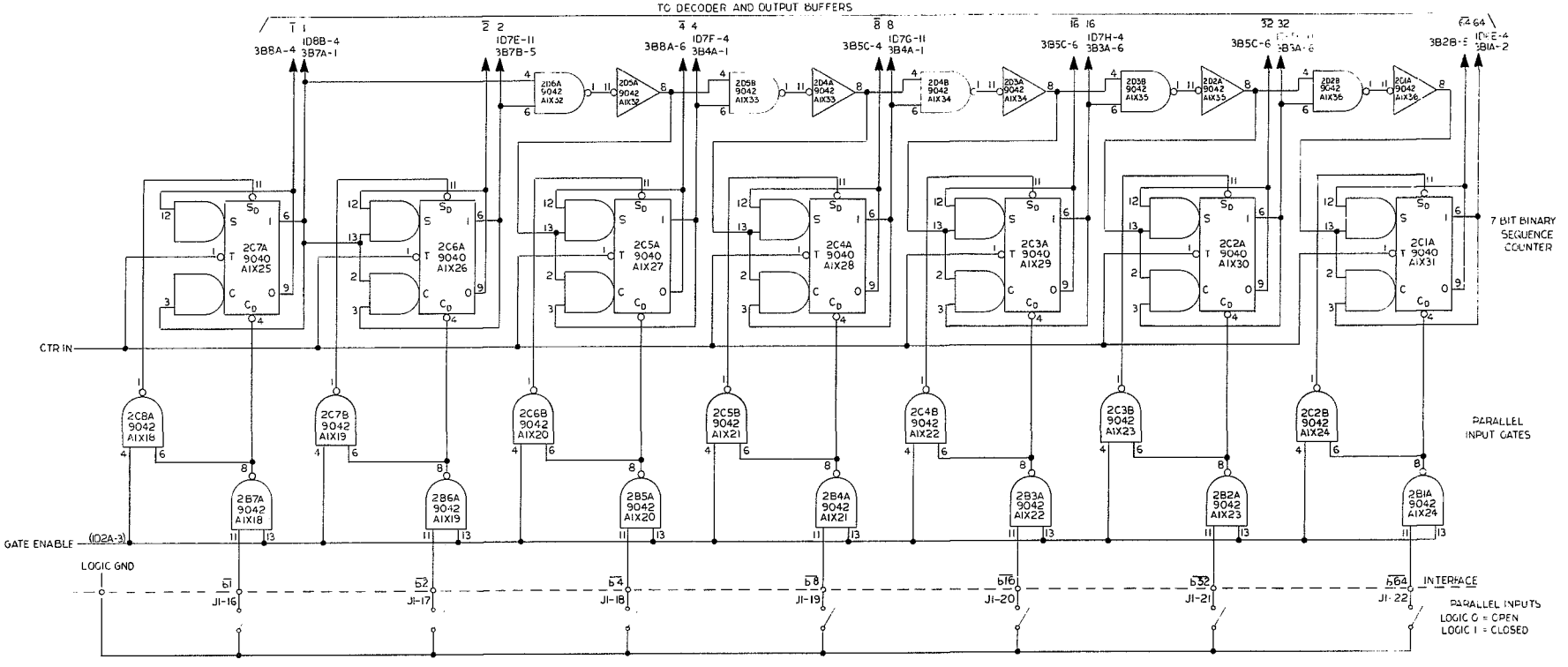


Figure 14. Binary Sequence Counter Logic

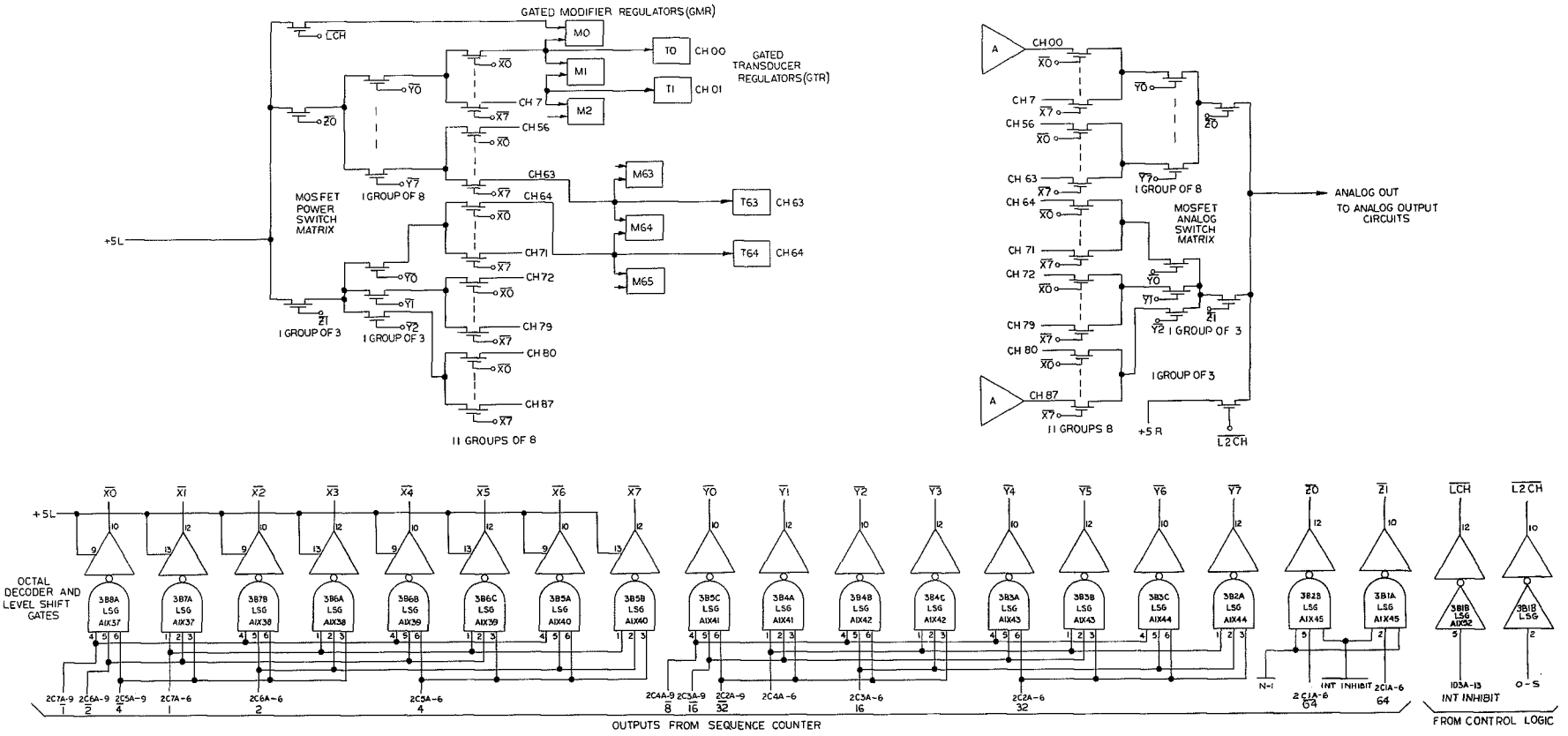


Figure 15. Octal Decoder Logic

while the last, most significant bit is converted to lines labeled Z0 and Z1. By combining one X line, one Y line, and one Z line in an AND arrangement, such as is done in the switch matrices, it is possible to decode the original sevel bits into 128 unique lines.

2.3.4 Parallel Input Control

The sequence counter is controlled from either parallel or serial inputs. When operating in the parallel mode, the serial input is inhibited and all changes to the state of the sequence counter must occur by jam-setting (forcing the counter to assume a selected one/zero code) to the desired channel number as determined by the parallel input gates. These gates are used to transfer a 7-bit input code into the counter whenever the GATE ENABLE line is energized. In the parallel mode of operation, the GATE ENABLE line is activated whenever the PARALLEL LOAD line is activated, and in this capacity serves as a strobe on the input lines, thus preventing unwanted switching transients from adversely affecting the sequence counter. The absence of the strobe also serves to disconnect the parallel input lines from the counter in cases where the input lines are changing, but is is not desired to change the state of the counter.

2.3.5 Sequential Start-Stop Control

In the sequential (or serial) mode of operation, the sequence counter is advanced serially one channel at a time by performing a countdown of the trigger pulses occurring on the CTR INPUT line. The CTR INPUT line is logically equivalent to the CLK signal, except that it can be gated OFF by an internal or external inhibit line. Either internal or external clock pulses are used to generate the CLK pulse train, which, in turn, generates the CTR INPUT trigger pulses. Selection of clock sources is provided by choosing the proper logic level for the INT/EXT CLOCK line.

The outputs of the sequence counter are connected through buffer amplifiers to an external connector. Furthermore, the inputs to the N - 1 coincidence circuit are also made available at the external connector. Normally, external connections are made between the buffer amplifiers and the coincidence circuit. The coincidence circuit will generate three outputs (SYNC, $\overline{\text{INT INH}}$, RESTART) whenever its inputs are all equal and at their active level. This means that by proper selection

of external connections, the coincidence circuit can be made to generate its outputs on any channel corresponding to the code provided by the buffer amplifiers. The SYNC output is used by the strobe circuit and the analog output circuits in order to generate the required PAM format. The $\overline{\text{INT INH}}$ output is used to inhibit the CTR IN signal during the time interval set aside for jam-setting the counter from the parallel input gates. The RESTART output serves the same purpose during serial operation as the PARALLEL LOAD line does dur ng parallel operation; it generates the GATE ENABLE signal which in turn causes the counter to set to the code connected to the seven input lines of the parallel input gates. This action occurs during the time interval corresponding to the second channel after that selected by the N - 1 coincidence circuit. To illustrate this operation, suppose the binary code for channel 88 is connected to the N-1 coincidence circuit, and the code for channel 00 is connected to the parallel input gates. Then, the operation is as follows: The sequence counter will advance to channel 88 (the Nth - 1 channel), continue on to channel 89 (the Nth or stop channel), and then restart on channel 00 (the Nth + 1 or start channel). It will continue to advance one channel at a time from 00 to 89 and then repeat the cycle. Thus, by programming the binary code at the inputs to the N - 1 coincidence circuit and the parallel input gates, the programmer can be made to scan any number of channels between a selected start channel and a selected stop channel.

2.3.6 Strobe Circuit

The strobe circuit generates the STROBE command fed to the analog output circuits. Its function is to sample the analog data during the time that it is in its active state. For the PAM format, this occurs during the second half of the each allotted channel period. For other formats, the strobe may vary from this 50 percent duty cycle. It is the function of the strobe circuit to permit maximum flexibility in selection of the proper strobe circuit.

The strobe circuit consists of an OR gate and a strobe select logic. The OR gate combines the CLK signal (which may be generated either internally or externally as described earlier) with the SYNC signal

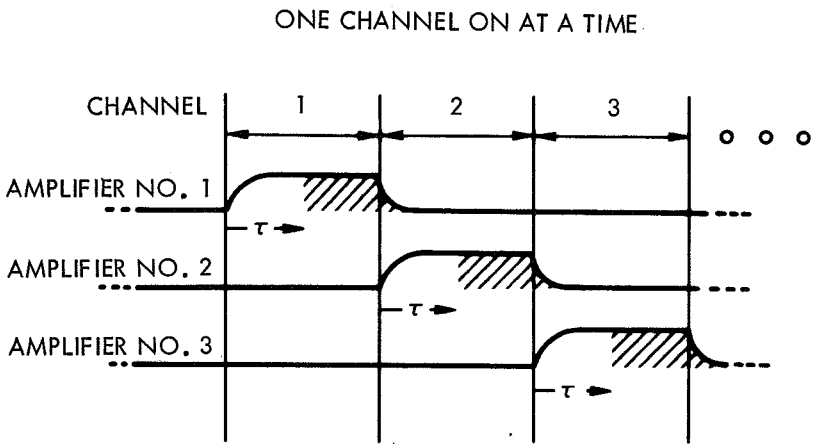
(active during the last half of channel N - 1 and both halves of channel N) in order to provide the signal INT STROBE. The SYNC signal is required in order to be compatible with PAM measurements. The strobe select logic produces the strobe output signal which is logically equivalent to either the INT STROBE or to an externally connected EXT STROBE signal. Selection of strobe sources is provided by choosing the proper logic level for the INT/EXT STROBE line. An additional input to the strobe select logic will override the internal or external strobe and produce a steady active output for the strobe line. This permits sampling analog data on a 100 percent basis.

2.4 SYSTEM SPEED AND POWER

Gating ON a signal modifier and/or a transducer one channel time in advance will triple the maximum switching rate at the expense of 43 percent increase in power. This relationship of speed and power is illustrated in Figure 16.

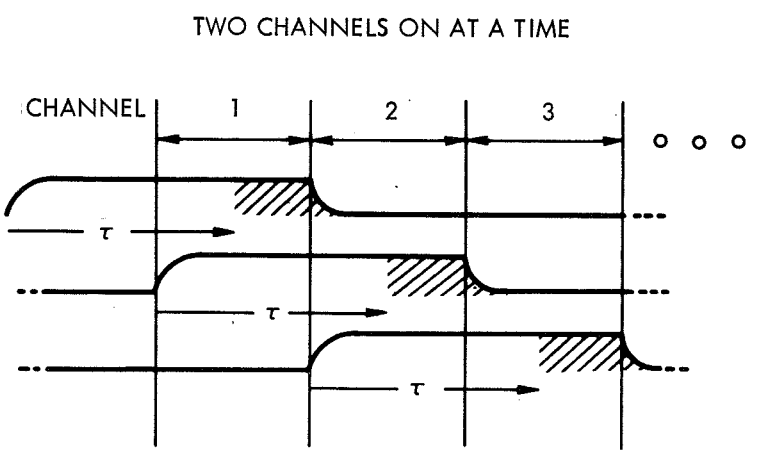
The signal modifier is assumed to stabilize within either 150 sec or 15 sec depending on the bandwidth selected; 10 kHz or 100 kHz, respectively. (See Section 2.2.2.) The primary disadvantage of the 100 kHz bandwidth is the resultant noise. With reference to Figure 16, note that a 100 kHz maximum switching rate is obtainable. This high switching rate may be particularly useful in a PCM adaptation of the Power Programmer. An IRIG specified PAM wavetrain requires a low switching rate of 900 Hz. In this application the Power Programmer does not require a channel to be turned ON in advance. Figure 16 also indicates the input power-speed relationship. The system power budget is shown in Table VI.

The maximum switching rate is controlled by the amplifier settling time. The specified setting times assume the Power Programmer in the sequential mode of operation. If an amplifier is switched ON in the parallel (or random access) mode, the settling time may be as great as 1 to 5 minutes due to long thermal time constants. In the sequential mode, however, a thermal steady state condition is obtained, allowing the settling times to be reduced to 15 sec for a 100 kHz bandwidth.



τ≡TOTAL AMPLIFIER SETTLING TIME
CROSSHATCHED TIME ≡ SAMPLE PERIOD

τ^*=	150 μ SEC	15 μ SEC
2τ =	300 μ SEC	30 μ SEC
MAX RATE =	3.3KHz	33KHz
POWER IN =	4500 MW	4500 MW



τ≡TOTAL AMPLIFIER SETTLING TIME
CROSSHATCHED TIME ≡ SAMPLE PERIOD

τ^* =	150 μ SEC	15 μ SEC
4/3 τ =	200 μ SEC	20 μ SEC
MAX RATE =	10 KHz	100 KHz
POWER IN =	6460 MW	6460 MW

*SEE TABLE II IN SECTION 2.2.2

Figure 16. Switching Rate vs. Power In

TABLE VI. SYSTEM POWER BUDGET

	Case 1 One GTR ON One GMR ON	Case 2 Two GTR ON One GMR ON	Case 3 Two GTR ON Two GMR ON
Transducer	300 mw	600 mw	600 mw
GTR dissipation	215	395	395
GTR input	515	995	995
Signal modifier	180	180	360
GMR dissipation	125	125	175
GMR input	305	305	535
Output Circuit	380	380	380
LSG	185	185	185
Control Logic	230	230	230
Net Power	1615	2095	2325
Into Pre-regulators*	2700	3500	3880
Total Input Power**	4500 mw	5820 mw	6460 mw
Could be reduced to	(2200 mw)	(3000 mw)	(3380 mw)

*Assuming 60 percent efficiency

**Assuming 60 percent efficiency

With respect to Table VI, the system power input can be reduced in the following manner:

a) If negative feedback was applied to the power converter, the regulation performance would be significantly improved allowing the series preregulators to be removed.

b) The output circuit uses Fairchild 709 amplifiers (for expediency). If these amplifiers were replaced with 50 mw dissipation circuits (a TRW integrated amplifier modified for low power consumption), the input power to the output circuit could be reduced from 380 to 130 mw.

If the above modifications were made, the total power input for one GTR and one GMR ON at a time) could be reduced from 4500 mw to 2200 mw.

2.5 SYSTEM ERRORS

Table VII lists the system error components. The contract specifications consider components 1 and 2. The RMS and Peak Net Error is below the specified 1 percent error. The complete system includes components 3 and 4.

TABLE VII. SYSTEM ERRORS

Item	Component	RMS Error (%)	Peak Error (%)
1	Analog Switches	0.17	0.2
2	Output Circuit	0.36	0.76
	Net Error	0.40	0.96
3	Transducer Excitation	0.5	0.5
4	Signal Modifier	1.4	1.4
	Total System Error	1.5	

3. CIRCUIT DESIGN

3.1 GATED REGULATORS

3.1.1 Circuit Principles

This section describes the circuit mechanization and the integrated circuit design of the functional block described and specified in Sections 2.2.3 and 2.2.4. The following discussion applies to both the GTR and GMR, since the organization of both circuits are similar. Figure 17 shows the general circuit approach used to meet the specifications.

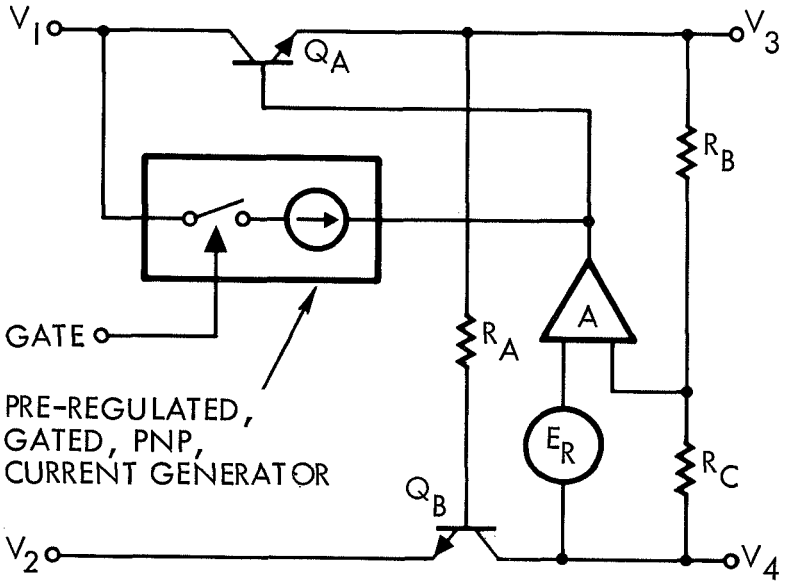


Figure 17. Grated Regulator Circuit Organization

Differential amplifier, A, maintains the junction of R_B and R_C at a reference voltage by controlling the base voltage of Q_A. Conventional regulators use a resistor from the base of the series regulating element, Q_A, to the positive supply potential, V_1. Instead, a pre-regulated PNP-current generator replaces this resistor for three reasons:

a) A PNP-current generator offers ease in gating, with the additional feature of the input power approaching zero during the OFF state. This is necessary to minimize the total system power input.

b) For given bias conditions, the dynamic collector impedance of the current generator is considerably larger than a conventionally used resistor. The feedback loop gain, which is directly proportional to this impedance, is therefore increased.

c) The preregulation aspect of this current generator further isolates the remaining circuit from the effects of input line voltage variations, thereby increasing the line regulation.

Transistor, Q_B, is a saturating switch which disconnects the negative line during the OFF state. Resistor R_A supplies base current only when the regulator is ON. Thus when the gating signal turns the current generator OFF, both Q_A and Q_B are turned OFF.

Figure 18(a) shows the preregulated, gated, PNP-current generator. The output current is controlled by the voltage across R_D, which is approximately equal to the voltage across R_E. The forward biased emitter-base junction of Q_D is used for temperature stabilization. The reverse emitter-base breakdown voltage of Q_E stabilizes the voltage across R_E and R_F, and therefore regulates the output current against changes in input line voltage. The current generator is ON only when the switch is closed, which in turn is controlled by the gating signal.

A lateral geometry, side-injection PNP transistor is used in the monolithic integrated regulator circuit because of the relative ease in fabricating the device in the same substrate with NPN transistors. However, the disadvantages of such a structure include low current gains ($\beta = 1 - 5$) and poor frequency response. Therefore, the composite structure shown in Figure 18(b) is used in place of Q_C because the effective β of the pair is the product of the β's of Q_F and Q_G.

The fabrication of the side-injection PNP transistor with buried layer epitaxial techniques presents difficulties in maintaining low substrate leakage currents and low substrate parasitic PNP β's. To circumvent these problems, the dielectric isolation process was selected as the appropriate technique for regulator substrate fabrication. A common substrate type (MCD3) is used for all regulators. Each regulator circuit type is fabricated by applying unique resistor and interconnect masks to the dielectrically isolated MCD3 substrate (see Section 4.2.2).

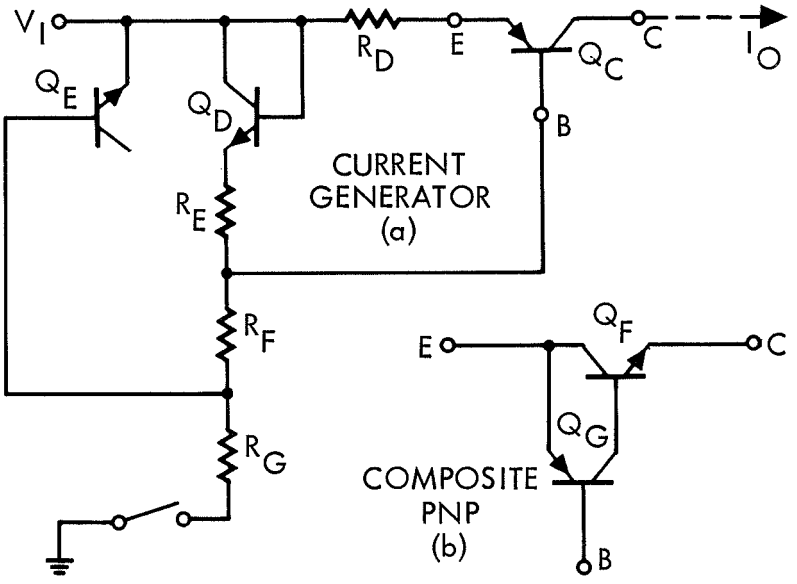


Figure 18. Regulator Current Generator Schematic

3.1.2 Gated Transducer Regulator

The gated transducer regulator schematic is shown in Figure 19. Logic gating signals are applied to P2 and/or P3. If either Q_4 or Q_5 are turned on, the PNP-current generator is turned on. (Note that numerous fuse links, which are shown on the schematic, must be blown before the regulator can be gated. It will be assumed that these links are open.)

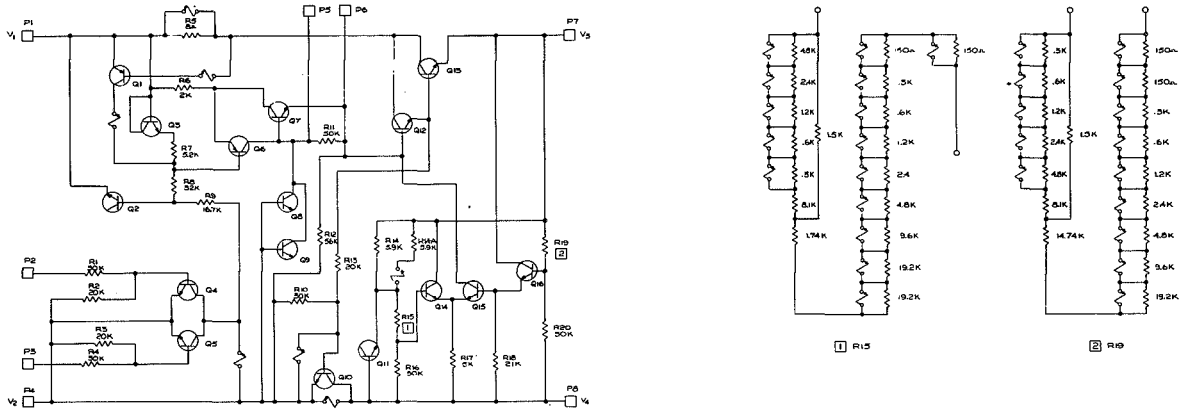


Figure 19. Gated Transducer Regulator Schematic

Transistor Q_1 monitors the voltage across the resistor R_5. Q_1 is normally OFF, but during an overcurrent condition, Q_1 will start to turn on, thereby turning off the current generator. This limits the short circuit current to a value approximately double the nominal current level.

Resistor R_{11} is included in the composite PNP structure (Q_6 and Q_7) to minimize the turn-off time. Transistor structures Q_8 and Q_9 are used as roll-off capacitors to dynamically stabilize the closed loop feedback circuit. Emitter follower, Q_{12}, drives the series regulating transistor, Q_{13}. Transistor, Q_{10}, is turned on and off via the current provided by R_{13}. This resistor is connected to the emitter of Q_{12} to stabilize and increase the operating current of Q_{12}.

The emitter-base junction of Q_{11} is reverse biased and used as a voltage reference diode. The typical parameter distributions are

$$BV_{BEO} = 6.5 \text{ to } 9.5 \text{ volts} \tag{3}$$

$$\frac{\partial BV_{BEO}}{\partial T} = 3 \text{ to } 5 \frac{mv}{^{o}C} \tag{4}$$

Resistive divider, R_{15} and R_{16}, is adjusted to develop a voltage temperature coefficient at the base of Q_{14} which is exactly equal and opposite to the temperature coefficient of the forward-biased emitter-base junction of Q_{16}. This establishes the base voltage of Q_{16} constant with respect to temperature. The regulator output voltage is then adjusted precisely to 10.00 volts by increasing R_{19}. This procedure allows the output voltage temperature drift and offset to be independently selected, thereby simplifying the adjustment procedure.

Table VIII indicates typical performance data for the GTR. Section 5 includes measured data on the twelve GTR circuits used in the breadboard model. The temperature performance is limited only by the nonlinearities and resolution of the resistor adjustments. The circuit was designed to drive either a 350 ohm or a 175 ohm transducer. For the latter case, care must be given to the package thermal characteristics to insure proper performance at $+95^{o}C$.

Figure 20 shows the assembly drawing of the GTR integrated circuit which incorporates the dielectrically isolated MCD3 substrate (see Section 4 for further information on the substrates and the total processing sequence).

Q_{10} and Q_{13} are large geometry NPN transistors designed to accommodate the 60 ma load current demanded by the 175 ohm transducers. The lateral geometry of the three types of transistor structures are described in Section 4.2.2. The cermet resistor line widths are typically 0.6 mil with 0.8 mil spacing. The metal line widths are 1 mil.

TABLE VIII. GTR CHARACTERISTICS

Power	30 ma Load	60 ma Load
P_D (dissipated)	215 mw	395 mw
P_O (output)	300 mw	600 mw
P_I (input)	515 mw	995 mw
ξ (efficiency)	58%	60%

$$\frac{\partial V_O}{\partial V_I} \leq 2 \frac{mv}{volt}$$

$$\frac{\partial V_O}{\partial T} \leq 300 \frac{\mu v}{^oC}$$

$$\frac{\partial V_O}{\partial I_i} \leq 200 \frac{\mu v}{ma}$$

3.1.3 Gated Modifier Regulator

The gated modifier regulator schematic is shown in Figure 21. This circuit operates according to the GTR description in Section 3.1.2 except for the following points:

a) Both the positive and negative output voltages must collapse to zero potential during OFF. This is necessary to reduce the signal modifier power dissipation to zero during OFF.

   For this reason, the triple emitter follower cascade, Q_{12} - Q_{13} - Q_{14}, is needed to prevent the emitter-base junctions from going into breakdown during OFF. Diode Q_{16} is needed to prevent the base-collector junction of Q_{17} from being forward biased during OFF.

b) The output voltage and its temperature coefficient is controlled in a different manner. Q_{18} and Q_{19} provide a variable linear temperature dependent current into the junction of R_{15} and R_{16}. Adjustment is accomplished by increasing R_{17}, R_{16}, and/or R_{15}.

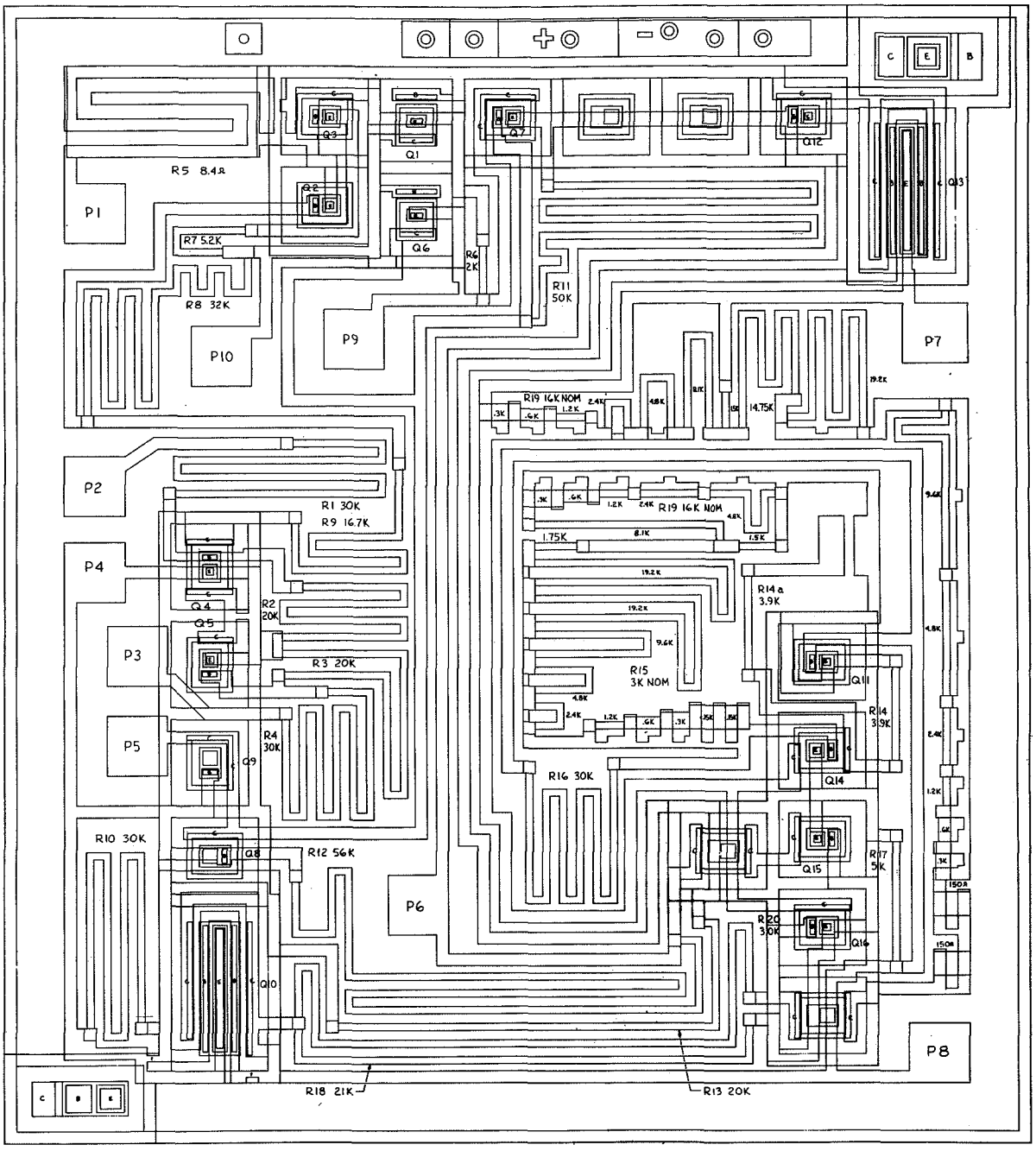


Figure 20. Gated Transducer Regulator Assembly Drawing

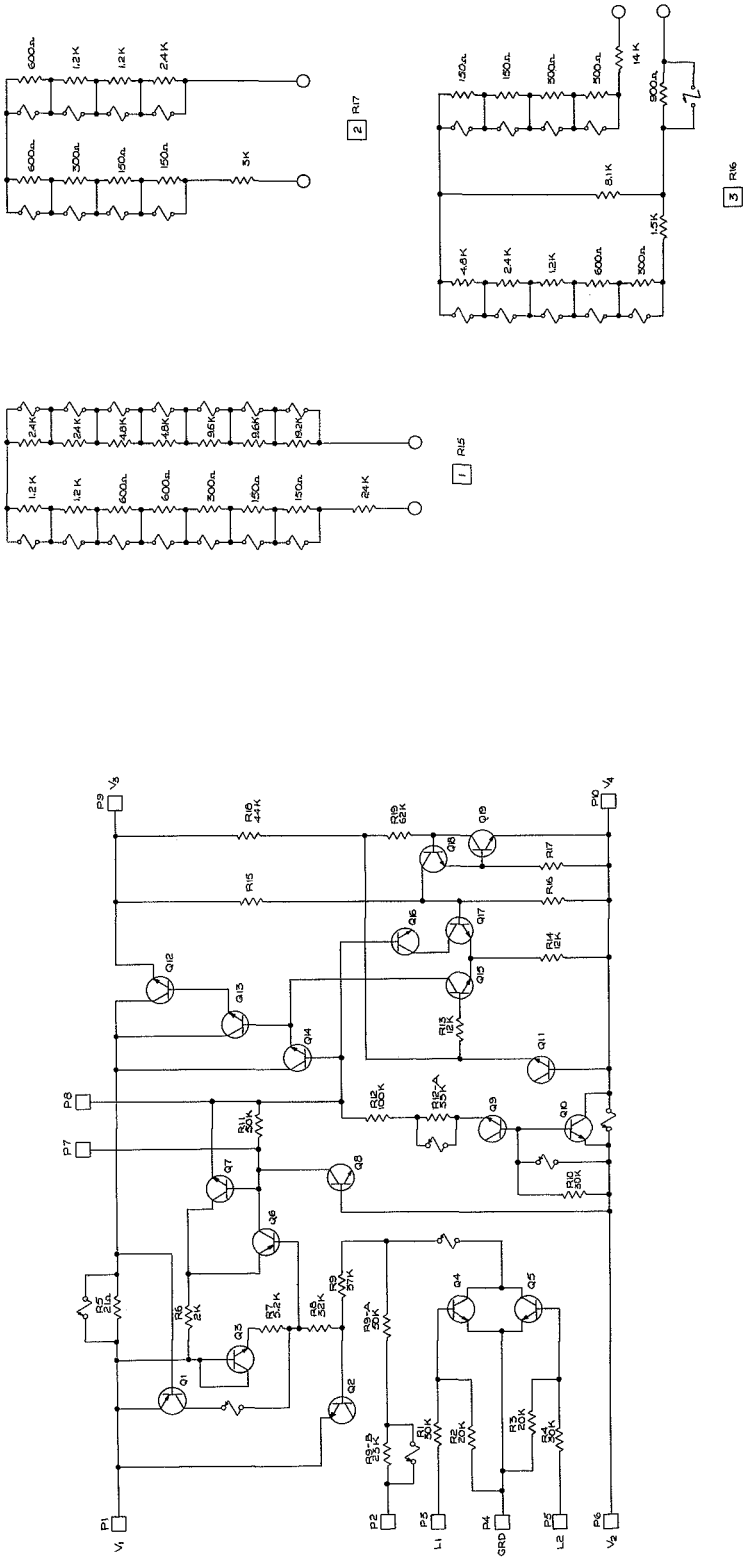


Figure 21. Gated Modifier Regulator Schematic

Table IX indicates typical performance data for the GMR. Appendix C includes measured data on the twelve GMR circuits used in the breadboard model.

Figure 22 shows the assembly drawing of the GMR integrated circuit which also incorporates the dielectrically isolated MCD3 substrate with evaporated resistors and aluminum interconnect. See Section 4 for further information on the substrates and the total processing sequence.

TABLE IX. GMR CHARACTERISTICS

P_D (dissipated) - 125 mw.

P_O (output) - 180 mw.

P_I (input) - 305 mw.

ξ (efficiency) - 59%

$$\frac{\partial V_O}{\partial V_I} \leq 4 \frac{mv}{volt}$$

$$\frac{\partial V_O}{\partial T} \leq 3 \frac{mv^*}{^oC}$$

$$\frac{\partial V_O}{\partial I_i} \leq 1.5 \frac{mv}{ma}$$

3.2 SWITCH MATRIX

3.2.1 MOSFET Integrated Switch

The MOSFET transistor was chosen as the switching device in the analog switch matrix described in Section 2.2.6 because of the following MOSFET properties:

a) The source-to-drain offset voltage in the ON state is zero.

b) The source-to-drain OFF impedance is extremely high (being limited primarily by the semiconductor leakage currents).

*This number can be reduced to 500 $\frac{\mu V}{^oC}$ or better by further adjustment.

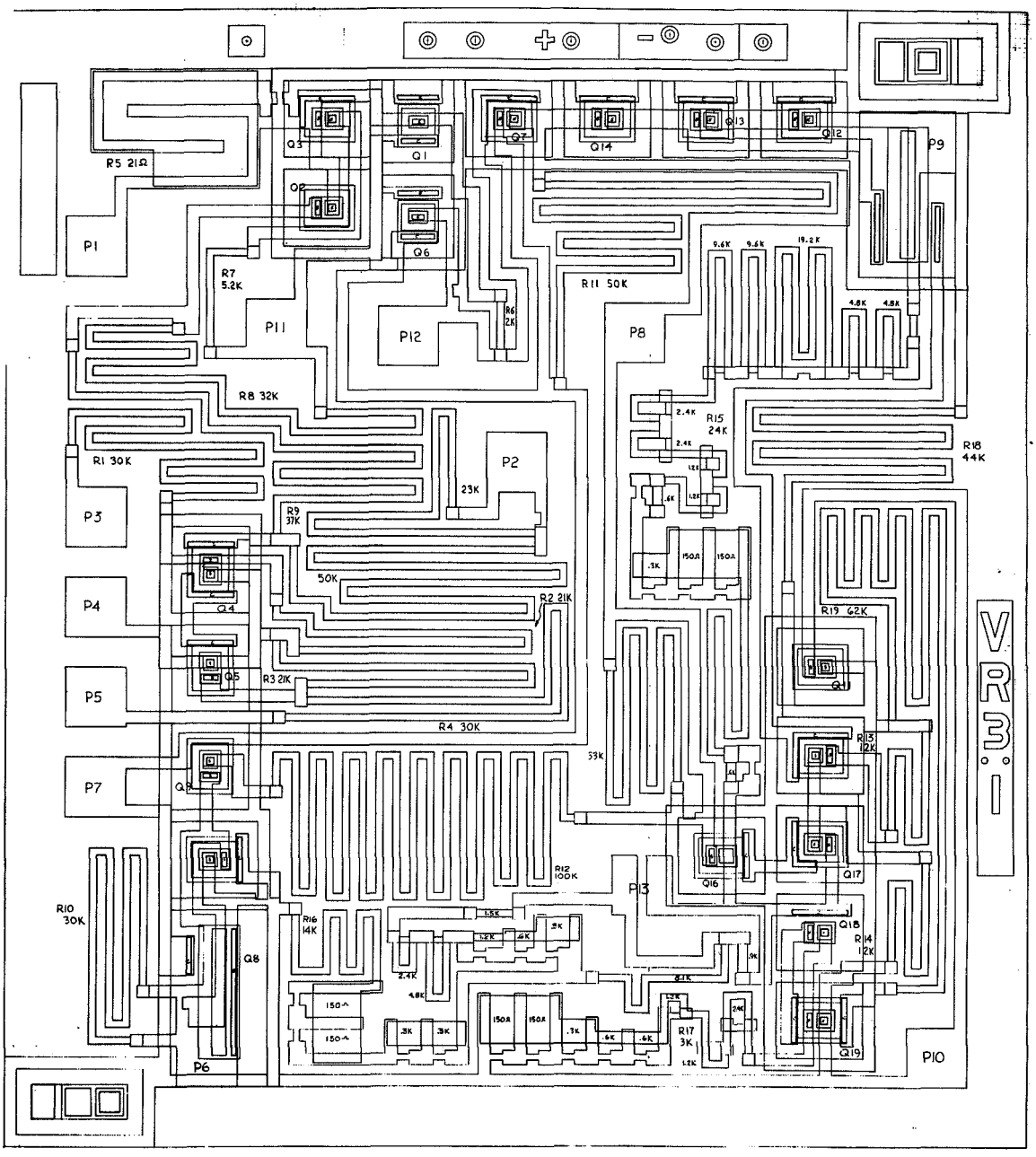


Figure 22. Gated Modifier Regulator Assembly Drawing

c) The gate is isolated from the source and drain by a silicon dioxide insulating layer. The gate input impedance is therefore extremely high ($>10^{10}$ ohms), thereby providing a high degree of isolation between the analog signal path and gate control voltage.

The same device was chosen for the power switch matrix because of the compatibility of logic control signals. Figure 23 is the schematic representation of the integrated five p-channel enhancement mode MOSFET transistor array. The drains are connected in common with the sources and gates brought out separately. The Zener diodes connected to the gates protect the MOS devices from catastrophic gate breakdown due to accumulated static charge.

Figure 24 shows the integrated circuit assembly drawing of the MOSFET array. Note that the protection diodes are placed just below the top row of interconnection pads. P_2 is used to make contact with the substrate via the top of the die. Pads P_4, P_6, P_8, P_{10}, and P_{12} are gates. Pads P_3, P_5, P_7, P_9, and P_{11} are sources. P_{1A} and P_{1B} are the common drain connection. The small pad near the MM-1 identification mark is used to measure the breakdown characteristic of the gate.

The measured minimum/typical/maximum parameters are compared with the system design specifications in Table X. Note that every measured worst-case parameter is better than the specified value. The following definitions apply to Table X:

V_{DS} ≡ DC drain-to-source voltage at saturation

$V_{DS(ON)}$ ≡ Drain-to-source ON resistance

BV_{DSS} ≡ Drain-to-source breakdown

BV_{GSS} ≡ Gate-to-source breakdown

BV_{SDS} ≡ Source-to-drain breakdown

V_{GST} ≡ Gate source threshold voltage

I_{DSS} ≡ Drain leakage current

I_{SDS} ≡ Source leakage current

I_{GSS} ≡ Gate leakage current

TABLE X. SUMMARY OF TEST DATA - MOSFET'S FOR USE IN MMG GATE CIRCUIT

Characteristic	Conditions ($T = 25^{\circ}C$ unless noted otherwise.)	Specification	Measured Values: Minimum	Typical	Maximum
$V_{DS(offset)}$	I_D = -100na	≤500μv			Note 1
$r_{DS(on)}$	V_{GS} = -15V, I_{DS} = -100μA	≤500Ω	250Ω	350Ω	450Ω
BV_{DSS}	I_D = -10μA, V_{GS} = 0	≥30 v	35 v	40 v	45 v
BV_{GSS}	I_{GS} = -10μA, V_{DS} = 0	≥30 v	Note 3		
BV_{SDS}	I_S = -10μA, V_{GD} = 0	≥30 v	35 v	40 v	45 v
V_{GST}	V_{GS} = V_{DS}, I_D = -10μA	≥3 v	3.45 v	3.6 v	5.0 v
I_{DSS}	V_{DS} = -5V, V_{GS} = 0, T = 105°C	≤500 na	56 na	75 na	82 na
I_{SDS}	V_{SD} = -5V, V_{GD} = 0, T = 105°C	≤500 na	45 na	60 na	82 na
I_{GSS}	V_{GS} = -15V, V_{DS} = 0, T = 105°C				Note 1
C_{SSb}	V_{SSB} = -1V, V_{GSB} = V_{DSB} = 0	≤5 pf	3.09 pf	Note 4	3.58 pf
C_{dsb}	V_{DSB} = -1V, V_{GSB} = V_{SSB} = 0	≤5 pf	3.22 pf	Note 4	3.26 pf
C_{gsb}	V_{GSB} = -1V, V_{SSB} = V_{DSB} = 0	≤5 pf	3.26 pf	Note 4	3.86 pf
g_{FS}	V_{DS} = -10, V_{GS1} = -10, V_{GS2} = -11, $\Delta V_{GS} = V_{GS1} - V_{GS2}$	Not Req'd	1200 μmhos	1700 μmhos	2200 μmhos

Notes:
1. Values negligible; too small to measure on existing equipment
2. Substrate connected to GND for all tests.
3. Since actual breakdown is destructive, units were checked for breakdowns ≥ 35 volts.
4. Insufficient number of samples to determine typical values.

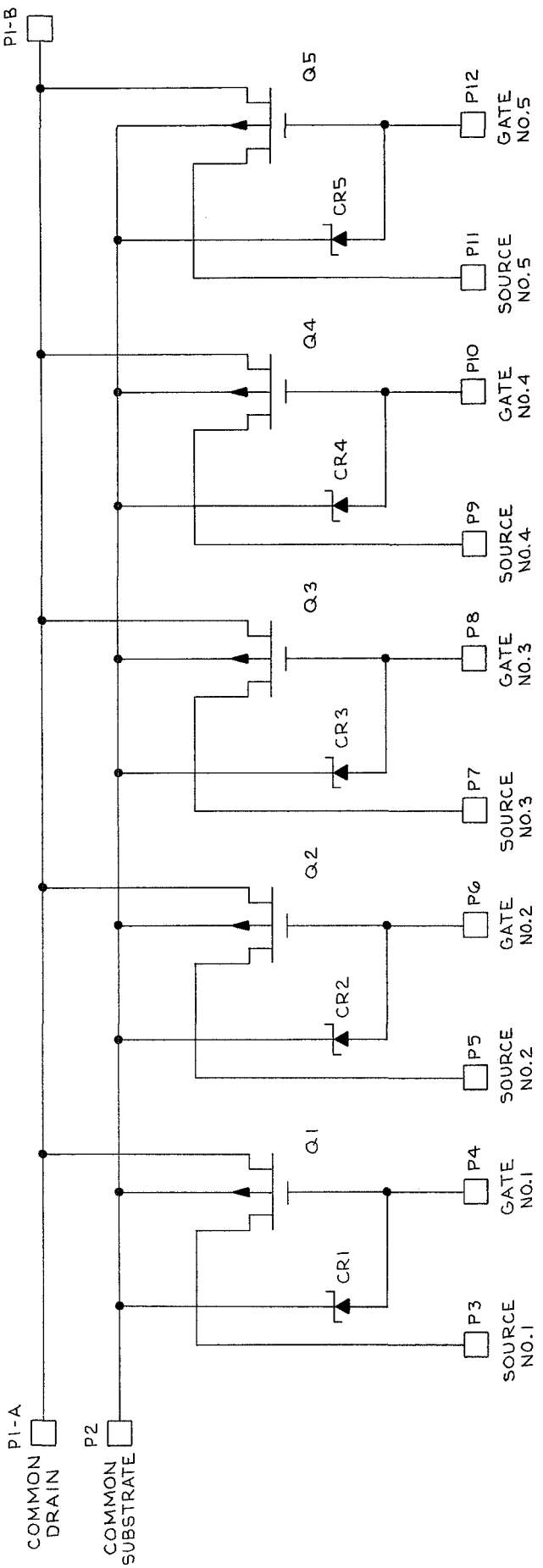


Figure 23. MOSFET Transistor Array Schematic

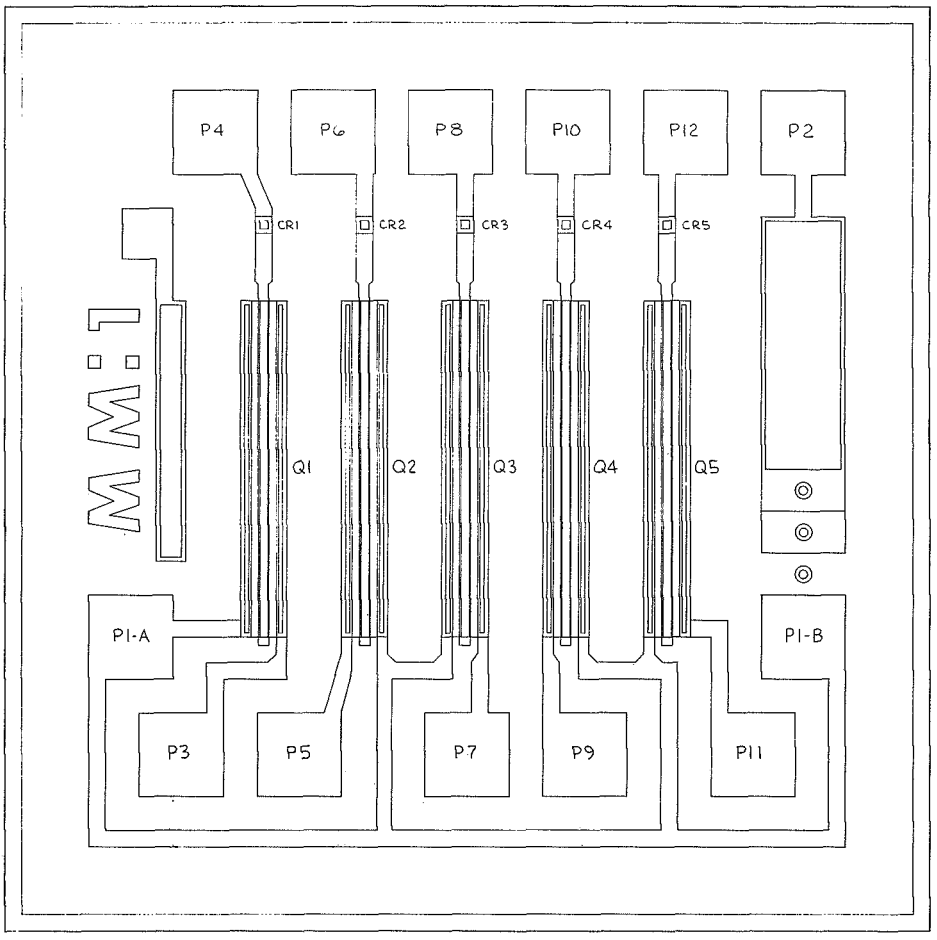


Figure 24. MOSFET Transistor Array Assembly Drawing

C_{SSb} ≡ Source-to-substrate capacitance

C_{dsb} ≡ Drain-to-source capacitance

C_{gsb} ≡ Gate-to-source capacitance

g_{FS} ≡ Transconductance

An equivalent circuit of the MOSFET is shown in Figure 25.

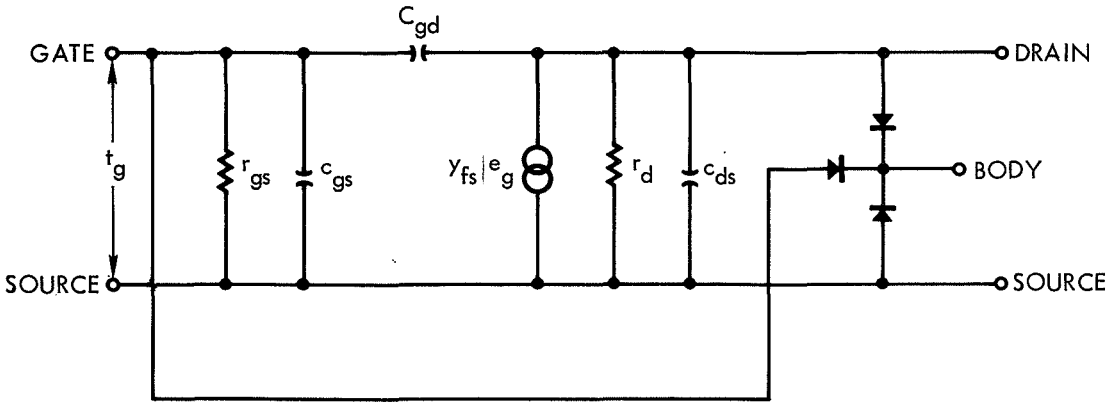


Figure 25. MOSFET Equivalent Circuit

3.2.2 Analog Application

Figure 26 shows a section of the analog switch matrix which will be used to discuss the worst-case performance. The primary factors contributing to analog errors are offsets due to leakage currents and attenuation due to ON resistance. Assuming that Q_1, Q_2, and Q_3 are ON and all other MOSFET are OFF, the equivalent schematic of Figure 27 is used to calculate the worst-case offset due to leakage currents.

With reference to Figure 15, the five-channel MM-1 circuits are organized so that each group of eight devices in the X level and the associated Y level device are mechanized with two flat packs. The X and Y levels are therefore mechanized with 22 flat packages, with one unused device contributing to leakage currents for every two packages. This explains

the eight I_{SDS} current component. The Z level is mechanized by one MM-1 flat package, explaining the four I_{SDS} current component.

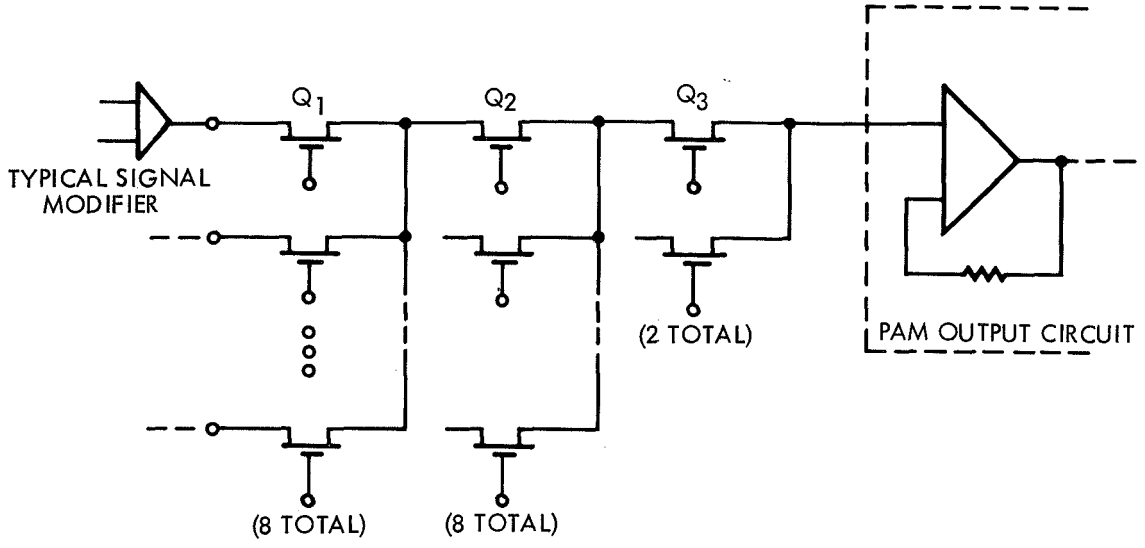


Figure 26. Section of Analog Switch Matrix

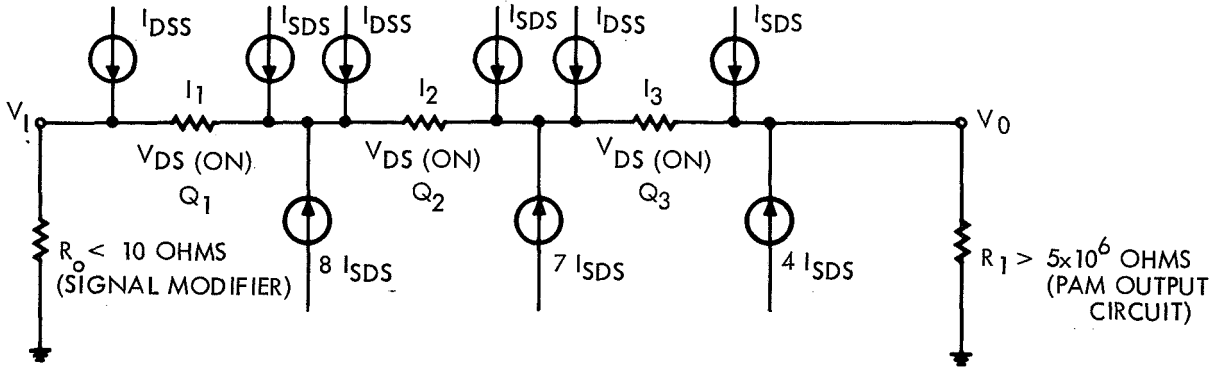


Figure 27. Worst Case Leakage Current Equivalent Circuit

The worst-case offset error voltage caused by leakages (at 105°C) is expressed as:

$$\Delta V_\xi = \text{Offset error}$$

$$= I_1 V_{DS(ON)} + I_2 V_{DS(ON)} + I_3 V_{DS(ON}$$

$$= (I_1 + I_2 + I_3) V_{DS(ON)}$$

where

$$I_3 = I_{SDS} + 4I_{SDS} = 5I_{SDS}$$

$$I_2 = I_3 + 8I_{SDS} + I_{DSS} = 13I_{SDS} + I_{DSS}$$

$$I_1 = I_2 + 9I_{SDS} + I_{DSS} = 22I_{SDS} + 2I_{DSS}$$

such that

$$\Delta V_\xi = (40I_{SDS} + 3I_{DSS}) V_{DS(ON)} \tag{5}$$

assuming

$$\overline{I_{SDS}} = \overline{I_{DSS}} = 200 \text{ na at } 105^\circ C$$

$$\overline{R_{DS(ON)}} = 500 \text{ ohms}$$

$$\Delta V_\xi = 8.6 \text{ mv} = 0.17 \text{ error (with reference to a +5 volt full scale signal)} \tag{6}$$

The gain error due to resistive divider attenuation is expressed as:

$$G_\xi = \text{gain error, attenuation factor due to the analog switch matrix}$$

$$= \frac{R_1}{R_1 + R_0 + 3V_{DS(ON)}} \simeq \frac{R_1}{R_1 + 3V_{DS(ON)}} \tag{7}$$

$$= 0.997, \text{ assuming } R_1 \geq 5 \times 10^6 \text{ ohms}$$

$$V_{DS(ON)} \leq 500 \text{ ohms}$$

$$\text{Error due to } G_\xi = 0.03 \text{ percent} \tag{8}$$

The timing of the gate drive signals creates a short duration overlap (approximately 400 nanoseconds) as the analog switch matrix switches from one channel to the next. This overlap is desirable as it provides a consistently low source impedance for the PAM Output Circuit. If this

overlap did not exist, the PAM Output Circuit could lockup due to a transient open source impedance. The reason for this overlap is described in Section 3.2.3.

The issue of maximum commutating speed is covered in Section 2.4.

3.2.3 Power Application

Figure 28 shows an X-Y-Z level and function of the power switch matrix, together with the MOSFET drivers and the gated regulators.

3.3

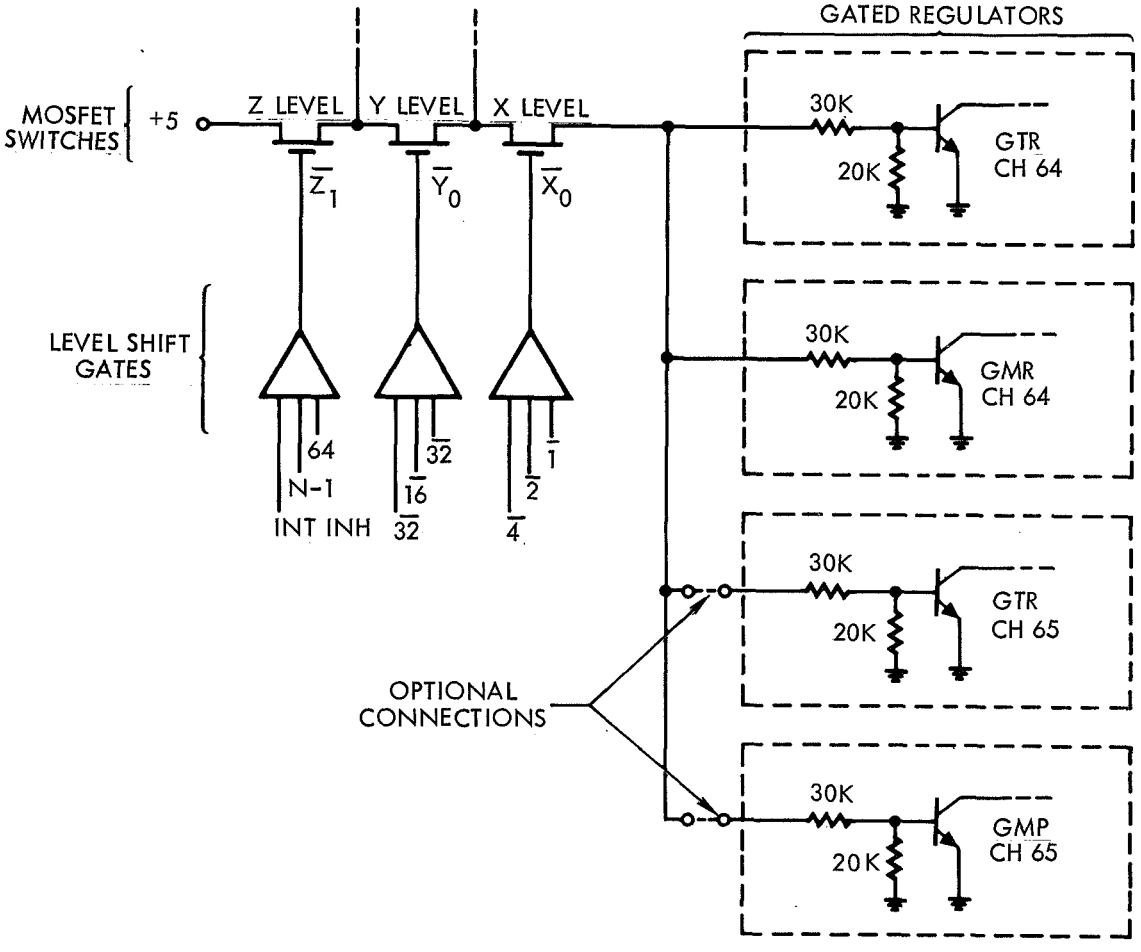


Figure 28. Section of Power Switch Matrix and Associated Circuitry

The circuitry associated with switching channel 64 is shown. Included is an option of simultaneously turning on channel 65 GTR and/or GMR regulators for preheating the next channel. This subject is discussed also in Section 2.4. Four gated regulators are shown because this represents a worst-case design configuration.

The resistor values were chosen, on the regulator gate inputs, to insure adequate base drive under conditions of:

a) +5 volt supply voltage minimum of +4.5 volts

b) Maximum MOSFET ON resistance of 1500 ohms

c) Minimum temperature of -40°C, producing maximum V_{BE} voltage

d) Maximum resistance values of 10 percent high

The turn-off time of the LSG circuit is approximately 400 nanoseconds longer than the turn-on time. There arises, therefore, cases in which crossover pulses turn on the regulators for a short period of time. (Pulses of a few microseconds duration are observed at the regulator outputs.) For instance, if the $\overline{Z}_1$ and $\overline{Y}_0$ lines are turning on while the $\overline{X}_0$ is turning off, there will be approximately a 400 nanosecond period in which all three MOSFET transistors are turned on. This overlap condition is not desirable in the power switch matrix, but it is needed in the analog switch matrix for reasons explained in Section 3.2.2. As long as these false ON pulses are very short duration, there will not be a significant increase in system power consumption or any operational fault. This condition is, therefore, not considered a problem.

3.3 CONTROL LOGIC

3.3.1 General Integrated Circuit Modules

The Power Programmer control logic is constructed using four basic digital building blocks. All four are manufactured by Fairchild Semiconductors and are available as off-the-shelf items. Two of the four, the 9040 flip-flop and 9042 dual NAND gate, are from the LPDTμL series specifically designed for low power applications, such as required by the Power Programmer. The other two, the 946 quad NAND gate and the 933 dual extender, are from the DTμL 930 series. The manufacturer's specifications for all four circuits are included as part of this report and contain all pertinent information as to pin connections, physical size, electrical

parameters, etc. The description that follows will therefore be limited to only those features which are not contained on the circuit specification sheets. In certain cases, sections of the specifications will be repeated, but only for clarification purposes.

3.3.1.1 9040, 9042 LPDTμL Circuits

The 9040 clocked flip-flop and 9042 dual 3-input NAND gate are both described in the composite LPDTμL low power diode transistor micrologic specification sheet. Page 2 contains the circuit diagram, pin connections, and truth tables for the clocked flip-flop. Page 4 contains similar data for the dual 3-input NAND gate. Both of these circuits utilize a modified DTL circuit as their basic element. The significant feature about these circuits is their power dissipation; the flip-flop dissipation is typically less than 4 milliwatts, while the NAND gate is typically less than 1 milliwatt. This property along with their excellent noise immunity (guaranteed greater than 450 millivolts) were the two main reasons for choosing the Fairchild LPDTμL series for use in the Power Programmer.

Operation of the NAND gate is such that if all three inputs are high (i.e., >3 v) the output voltage is low (i.e., < 0.5 v). Since the Power Programmer uses the positive logic convention, i.e., logic 1 = high voltage, logic 0 = low voltage, this means that the NAND gate output is at logic 0 only when all three inputs are at logic 1. If any one of the three inputs is at logic 0 (<0.5 v), the NAND gate output will be at logic 1 (>3 v). Note that because the circuit is constructed using the modified DTL circuit an input connection disconnected is the same as a logic 1. Thus, if one input is high and the other two inputs disconnected, the NAND output will be at logic 0.

The 9040 clocked flip-flop (see page 2 of specification sheet) is in reality two flip-flops connected in a "master-slave" combination. The flip-flop is capable of operation in either the J-K or R-S mode, both of which are described in the truth tables shown on page 2. The flip-flop will operate in either a synchronous or asynchronous mode. In the synchronous mode, data is entered through the Set (S_1, S_2) and Clear (C_1, C_2) gates. This is shown in Figure 29, which is a more detailed

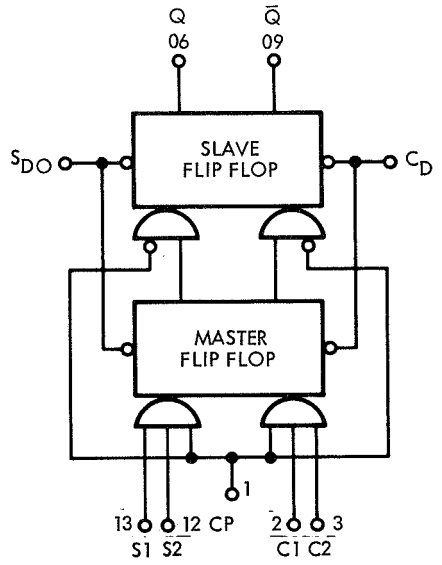


Figure 29. 9040 Clock Flip-Flop Schematic

drawing of the basic flip-flop symbol, as shown on page 2 of the specification. During the time the clock pulse (CP) is at logic 1, data on the Set and Clear inputs is transferred to the "master" flip-flop. When the clock pulse transition from logic 1 to logic 0 occurs, this data is transferred from the master flip-flop to the slave flip-flop. In the asynchronous mode, unclocked data is entered directly via the Set Direct (S_D) and Clear Direct (C_D) inputs. These inputs are activated when brought to the logic 0 level and will override the conditions present on the clocked inputs. Note a logic 0 on both inputs simultaneously is a forbidden condition.

3.3.1.2 946 Quad Gate

The 946 Quad 2-Input Gate is used in the Power Programmer as an output buffer or power NAND gate. Used as a power NAND gate, it can drive up to 24 LPDTμL circuits. As an output buffer amplifier, it has the capability of providing up to 10 milliamps of sink current to external circuits. Its logic operation is identical to that of the LPDTμL NAND gate, except that it has only two inputs instead of three.

3.3.1.3 933 Dual Extender

This circuit consists of two sets of four diodes, each set having its common anodes tied together. It is used to extend the number of input

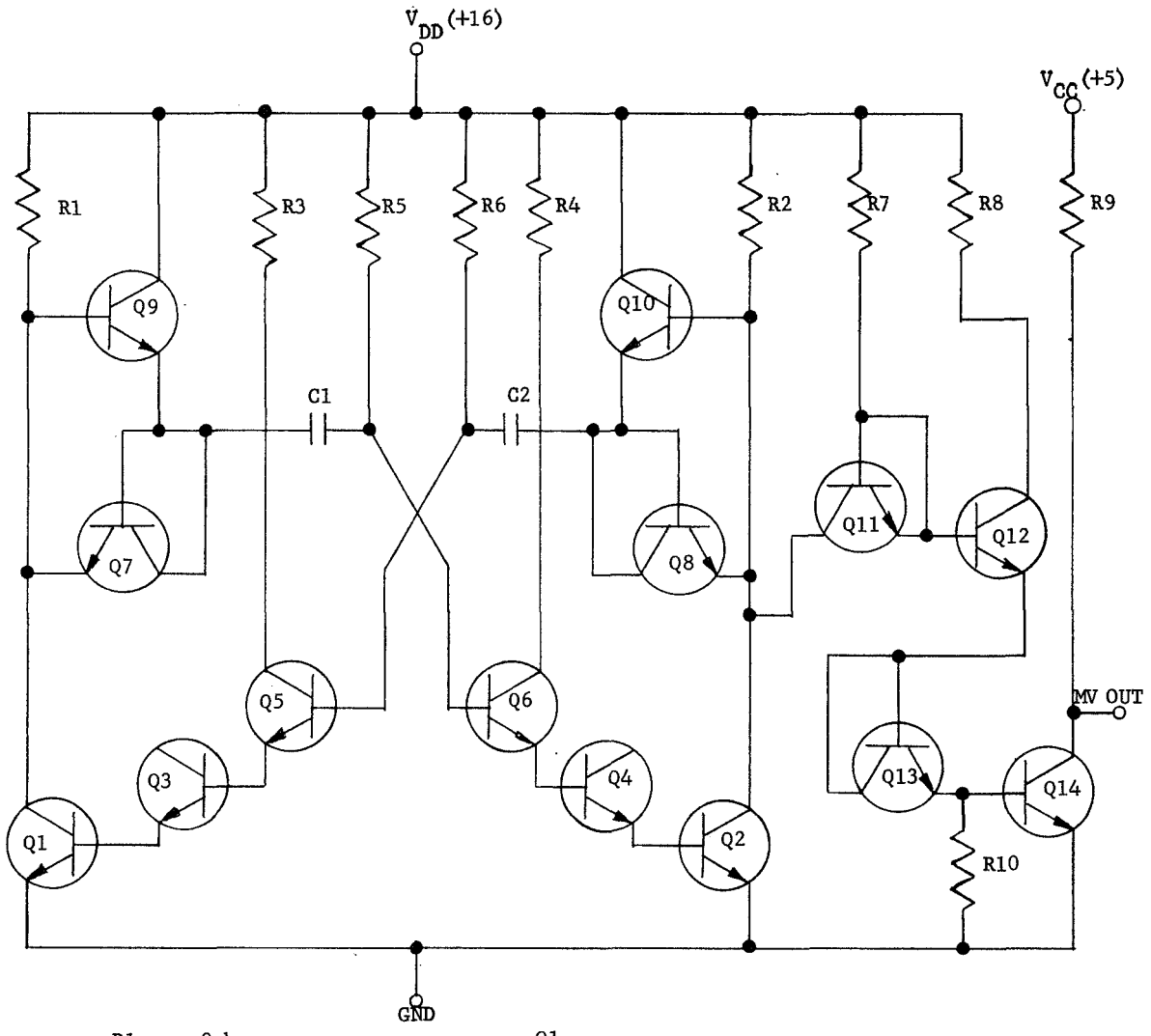
terms of the 9042 NAND gate. It is used only once in the Power Programmer, to extend the inputs to the N-1 Coincidence Circuit (see Dwg. X235498, Logic Diagram, Power Programmer). Complete specifications for the diode characteristics are given on the manufacturer's data sheet (see Appendix G).

3.3.2 Multivibrator Clock

Significant improvements in performance characteristics can be obtained by making relatively simple changes to a conventional astable multivibrator. The circuit illustrated in Figure 30 exhibits greatly improved temperature and power supply frequency stability while at the same time produces a longer time interval for the same capacitor size then a conventional multivibrator. In addition, power dissipation is minimized due to built-in emitter followers since waveforms are not deteriorated even with large values of collector resistors.

The circuit consists of a modified astable multivibrator coupled to an output buffer amplifier. The multivibrator operates as follows. Assume Q_1 on, Q_2 off. Q_2 will begin to turn on as soon as R_5 has charged C_1 to a voltage greater than the forward drop of three base-emitter diodes, (Q_2, Q_4, and Q_6). The voltage at the collector of Q_2 then decreases rapidly toward ground. This negative charge in voltage cuts off Q_{10} and, in addition, is coupled thru capacitor C_2 and diode-connected transistor Q_8 to the base of transistor Q_5. Since the base of Q_5 is more negative than ground, the base-emitter diodes of Q_5, Q_3, and Q_1 are reverse biased and Q_1 cuts off. Q_1 off enables R_1 to supply current to Q_9 which in turn supplies current thru C_1 to the base of Q_6. This current reinforces the original drive current through R_5, thus creating regenerative positive feedback. This condition will remain until R_6 charges C_2 to a voltage greater than the forward drop of the base-emitter diodes of Q_1, Q_3, and Q_5. At this point, Q_1 begins to turn on and the entire switching process is repeated, resulting in Q_1 on, Q_2 off, and so on.

Q_5 and Q_6 function as emitter followers which serve to increase the current gain and thus minimize the required drive current produced by R_6 and R_5, respectively. In addition Q_5's reverse base-emitter voltage



R1	9 k
R2	12 k
R3	57 k
R4	57 k
R5	120 k
R6	120 k
R7	39 k
R8	30 k
R9	9 k
R10	9 k
C1	3300 pF
C2	3300 pF

Q1, Q2	TA-01
Q3, Q4	TA-01
Q5, Q6	TA-01
Q7, Q8	TA-01
Q9, Q10	TA-01
Q11, Q12	TA-01
Q13, Q14	TA-01

Figure 30. Astable Multivibrator

breakdown, in series with that of diode Q_3 and the base-emitter of Q_1, is sufficient to prevent unwanted zener breakdown when the base of Q_5 is driven negative with respect to ground. The same argument applies to Q_6, Q_4, and Q_2. Q_9 and Q_{10} provide an active pull up to discharge C_1 and C_2 as rapidly as possible without consuming excessive power as in the case of low value Q_1 and Q_2 collector resistors. Diodes Q_7 and Q_8, in addition to providing a path for discharge of C_1 and C_2, help to minimize frequency changes with power supply and temperature variations by compensating the forward drop of diodes used elsewhere in the circuit. Transistors Q_{11}, Q_{12}, Q_{13}, and Q_{14}, along with resistors R_7, R_8, R_{10}, and R_9, are used to form a conventional DTL inverting amplifier. When the collector of Q_2 (i.e., the output of the multivibrator) is near ground, Q_{14} is off and the amplifier output is at V_{cc}. Conversely, Q_2 off turns Q_{14} on the amplifier output is at ground.

Stability of the multivibrator frequency with respect to temperature and power supply variations is achieved by use of diode compensation. This can be seen by observing the expression for the time interval during one-half of the multivibrator cycle. During the time interval when Q_1 is on, this expression is given by

$$T_1 = R_5 C_1 \ln \frac{2V_{cc} - \left[V_{BE2(sat)} + V_{BE4(sat)} + V_{BE6(sat)}\right]}{V_{cc} - \left[V_{BE2(th)} + V_{BE4(th)}\right]} - \frac{\left[V_{BE9(sat)} + V_{BE7(sat)} + V_{CE1(sat)}\right]}{+ V_{BE(th)}} \tag{9}$$

A corresponding equation can be written for T_2, the time interval when Q_2 is on. For symmetrical components, $T_1 = T_2$ and the overall frequency is simply

$$f = \frac{1}{T_{total}} = \frac{1}{T_1 + T_2} = \frac{1}{2T_1} \tag{10}$$

The important thing to note about Equation (9) is that for

$$V' = V_{BE2(sat)} + V_{BE4(sat)} + V_{BE6(sat)} \doteq V_{BE9(sat)} + V_{BE7(sat)}$$

$$+V_{CE1(sat)} \doteq V_{BE2(th)} + V_{BE4(th)} + V_{BE6(th)}$$

(A reasonable assumption considering all diodes and transistors are processed simultaneously.) Equation (9) then reduces to

$$T_o = R_5C_1 \ln \frac{2V_{cc} - 2V'}{V_{cc} - V'} = R_5C_1 \ln 2 = 0.694\ R_5C_1 \qquad (12)$$

The result is that the time interval T_1 is independent of both V_{cc} and V_{BE} voltages, depending only upon the values of R_5 and C_1. A similar condition exists for T_2; Thus the overall period T_{total} is dependent only upon R_5, R_6, C_1, and C_2.

This circuit was delivered in discrete component form.

3.3.3 Level-Shift Gate

The basic circuit configuration of the level-shift gate (LSG-05) is shown in Figure 31. The circuit is a dual, three-input modified DTL level shift NAND gate consisting of an input diode gate, a common-base PNP-NPN combination pair, level-shift stage, and an NPN output inverter. In addition to providing three-input gating, the LSG-05 is designed specifically for converting standard DTL logic levels into the levels required to drive the MOS multiplex gates. Since the output inverter is switched between +5V and -16V, the substrate must be biased at -16 volts.

Two output drive options are provided on the LSG-05 circuit. For cases where the load capacitance is small, the V_{xx} terminals are left open. This results in an output rise time dependent upon $(R_5 + R_6) \times C_G$. For larger load capacitance, and in cases where power consumption is not critical, the V_{xx} terminals are shorted to the V_{yy} terminal producing an output rise time dependent only upon $R_5 \times C_G$.

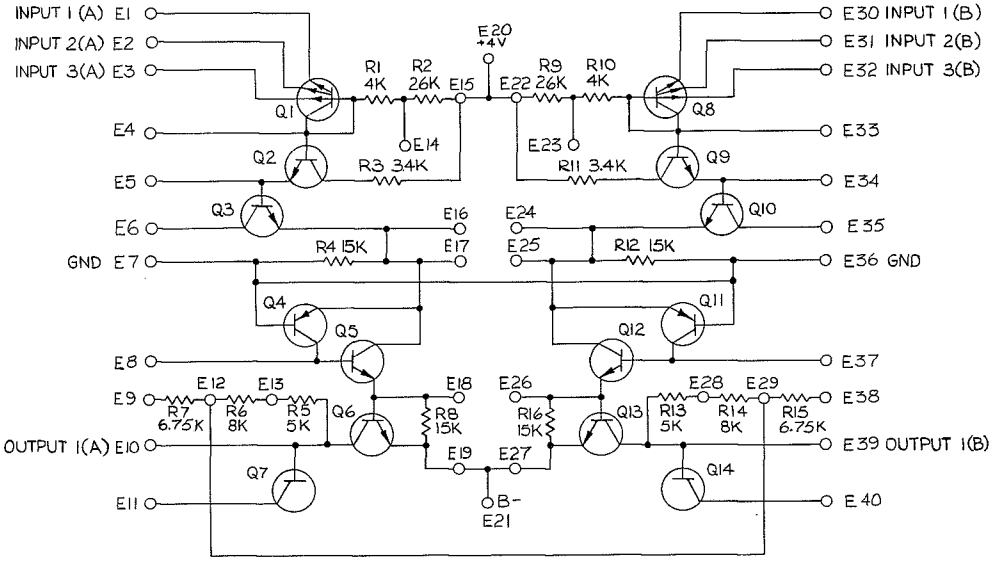


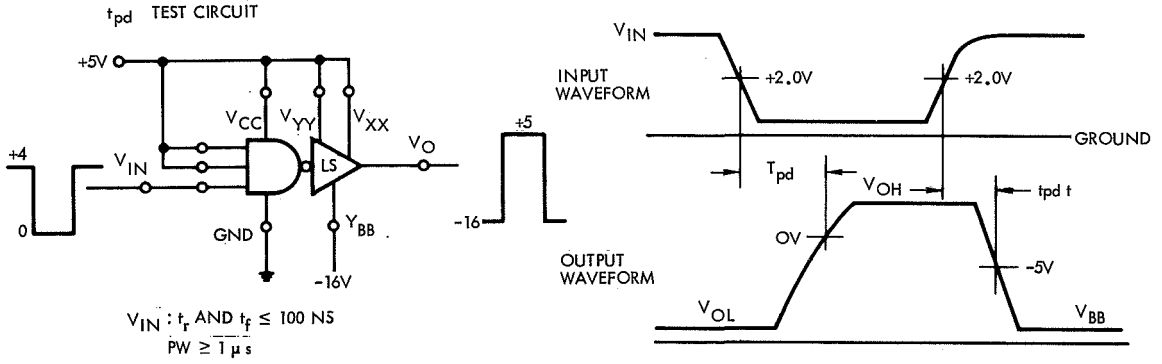
Figure 31. Level-Shift Gate (LSG-05) Schematic

Figure 32 shows the integrated circuit assembly drawing. The electrical specifications are included in Table XI.

The following definitions apply to Table XI.

V_{OL}	Output low voltage, with maximum current I_O into output
V_{OH}	Output high voltage, with maximum current I_O flowing out of output
I_R	Reverse input diode current with maximum input reverse voltage applied
I_F	Forward input diode current
I_{SC}	Short circuit output current to V_{BB}, with one or more inputs at GND
I_{VCXY}	Power supply current measured as sum of current into V_{cc}, V_{xx}, and V_{yy} pins when all three are tied together and all inputs are open
I_{VBB}	Power supply current flowing out of V_{BB} pin with all inputs open
$t_{pd}+$	See waveform below
$t_{pd}-$	See waveform below

The following drawing illustrates the test circuit and input-output waveforms:



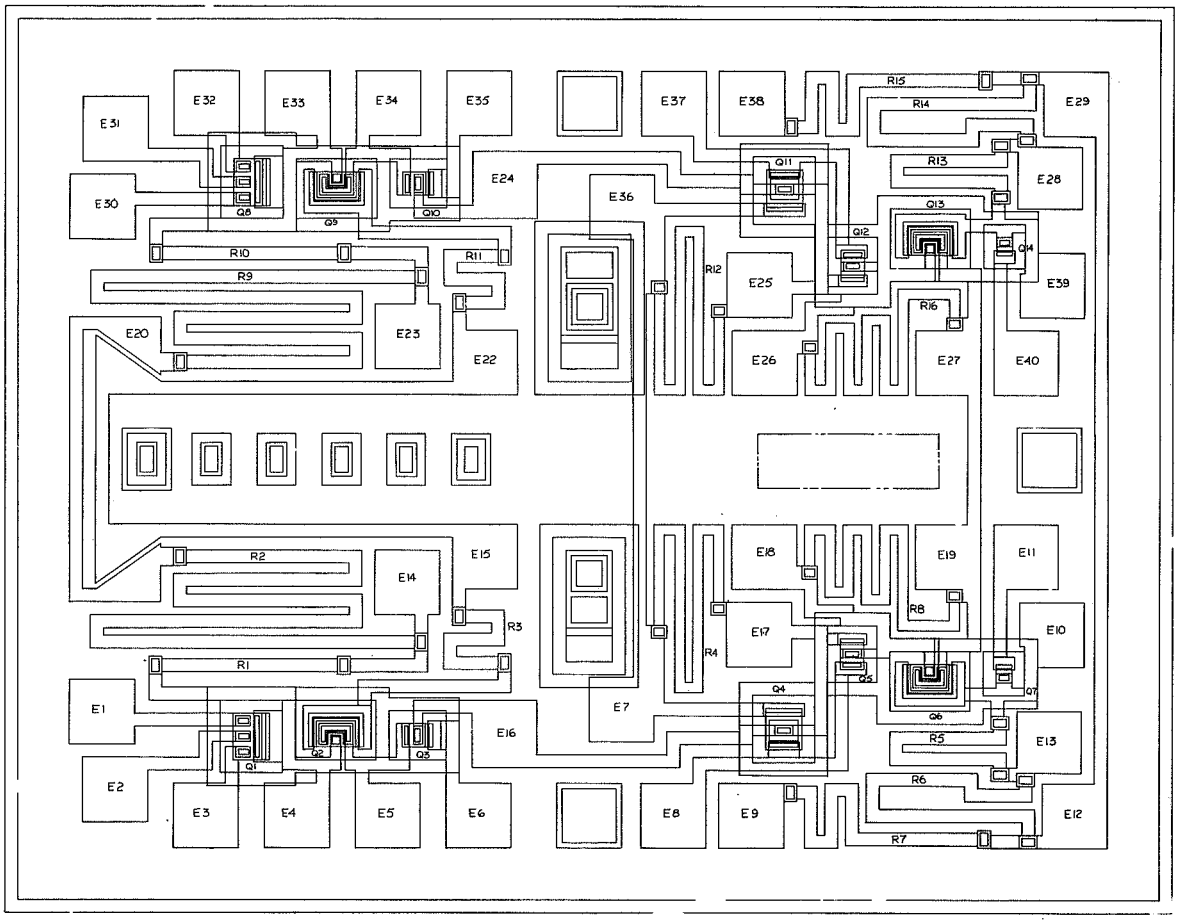


Figure 32. Level-Shift Gate (LSG-05) Assembly Drawing

TABLE XI. LEVEL SHIFT GATE ELECTRICAL SPECIFICATIONS

Test	Limits		Conditions							
Symbol	Min	Max	I_O	V_O	V_{cc}, V_{yy}	V_{XX}	V_{BB}	V_{IN1}	V_{IN2}	V_{IN3}
V_{OL}	-14.7V		+4 ma		+4.5V	+4.5V	-15.2	+2.5	+2.5	+2.5
V_{OH1}	+3.0V		-10 μA		+4.5		-16.8	+.45	+.45	+.45
V_{OH2}	+3.0V		-100 μA		+4.5	+4.5	-16.8	+.45	+.45	+.45
I_{R1}		10 μA			+5.5	+5.5	-16	+5.5	GND	GND
I_{R2}		10 μA			5.5	5.5	-16	GND	+5.5	GND
I_{R3}		10 μA			5.5	5.5	-16	GND	GND	+5.5
I_{F1}		0.2 ma			5.5	5.5	-16	GND	+5.5	+5.5
I_{F2}		0.2 ma			5.5	5.5	-16	+5.5	GND	+5.5
I_{F3}		0.2 ma			5.5	5.5	-16	+5.5	+5.5	GND
I_{SC1}	3.5 ma	5.2 ma		-16V	5.0	5.0		GND		
I_{SC2}	1.2 ma	2.0 ma		-16V	5.0			GND		
I_{VCXY}		6.5 ma			5.0	5.0	-16			
I_{VBB}		5.6 ma			5.0	5.0	-16			
t_{pd} +		300 ns (see test circuit)								
t_{pd} -		500 ns (see test circuit)								

Absolute Maximum Ratings (above which useful life may be impaired)

V_{CC} +8 volts continuous, +12 volts pulsed ≤1 sec

V_{XX} +12 volts continuous

V_{YY} +12 volts continuous

V_{BB} -20 volts continuous

Temperature: Unless noted otherwise, all specifications listed above apply over entire operating temperature range.

Operating temperature range: -55°C to +125°C

Storage temperature range: -65°C to +150°C

TABLE XI. LEVEL SHIFT GATE ELECTRICAL SPECIFICATIONS

3.4 PAM OUTPUT CIRCUIT

The PAM Output circuit schematic is shown in Figure 33. With reference to the waveforms and specifications given in Section 2.2.8, the functional description of the circuit schematic is as follows.

The input terminal (X, 20) accepts multiplexed analog signals from the analog switch matrix, such as shown in Figure 10(b). Amplifier number 1 is connected in a noninverting unity gain configuration to provide an input impedance greater than 100 megohms. The schematic and specifications of the microamp-709 amplifier, which was used in the breadboard model, are included in Appendix E. An amplifier with lower power dissipation is preferred since the PAM output circuit is operated continuously, but this model was used because of its availability.

Only 12 channels in the breadboard model have analog input connections; therefore, selection of channels other than the twelve presents an open circuit to amplifier number 1. On the breadboard, to prevent this amplifier from locking up, a 4.7 megohm resistor shunts the input to ground. This resistor would not be needed on a complete programmer since the source impedance of amplifier number 1 would always be low.

A 1K ohm resistor is included in the unity gain feedback loop to equalize the source impedances of both inputs, pins 2 and 3, thereby minimizing effects of base current drift. Two capacitors and one resistor are used for dynamic stabilization.

Two diodes are connected to the output of amplifier number 1 to limit the voltage swing to 0 through +5 volts. The 100 ohm resistor provides current limiting when either diode conducts. The 10.7K to 43.2K ohm resistors connected from the amplifier output to the +5 volt reference potential provide the algebraic manipulation described by Equation (1) in Section 2.2.8. The MOSFET transistors are series-shunt choppers driven by two LSG-01 level shift gates from the digital inputs of terminals (N, 12), R, 14), and K, 9). The MOSFET specifications are included in Section 3.3.1. The choppers are operated out-of-phase such that the input of amplifier number 2 is connected either to the analog input or to ground, Equation (1).

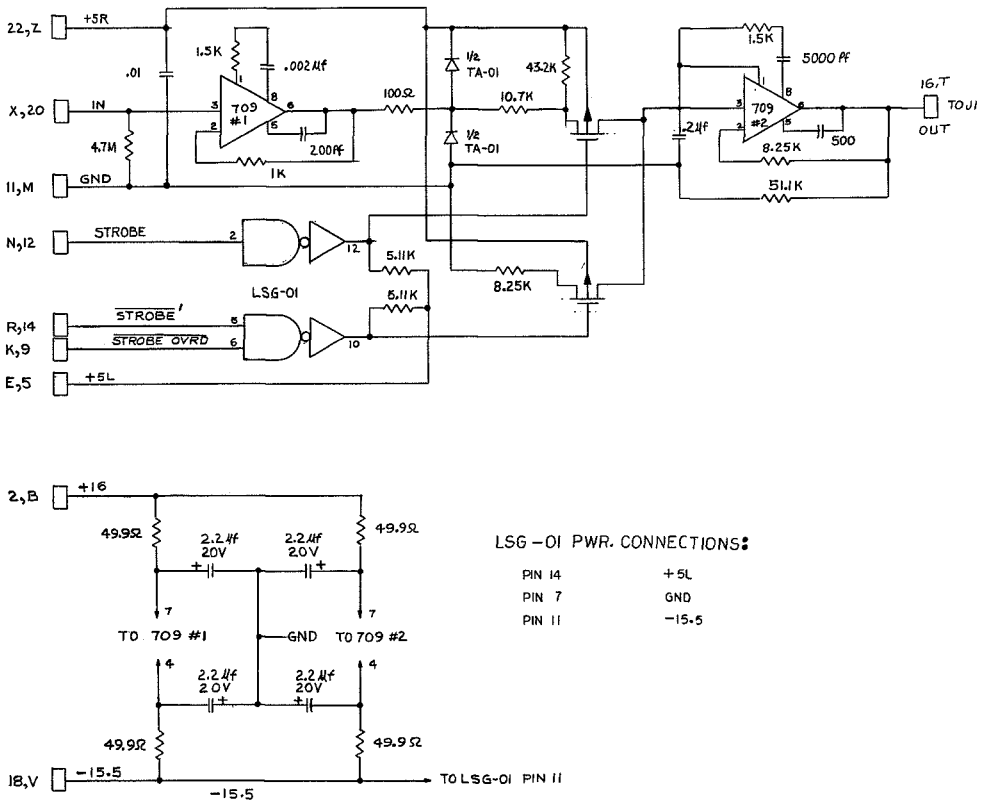


Figure 33. PAM Output Circuit Schematic

Amplifier number 2 is also a high input impedance noninverting unity gain circuit. The 8.25K ohm resistor is included in the unity gain feedback loop to equalize the source impedance of both amplifier inputs, thereby minimizing effects of base current temperature drift. Three capacitors and one resistor are used for dynamic stability. The output impedance as measured from terminal (16, T) is less than 0.01 ohm. The power supply lines of both amplifiers are decoupled to prevent instabilities. The maximum power supply current and power dissipations are given in Table XII.

TABLE XII. PAM OUTPUT CIRCUIT POWER SUPPLY REQUIREMENTS

Voltage	Current	Power Input
+16	11 ma	176 mw
-15.5	11 ma	171 mw
+5R	50 μa	- -
+5L	6.5 ma	33 mw
	Total	380 mw

The analog errors introduced by the PAM output circuit are itemized in Table XIII, assuming the specified system environment.

3.5 POWER SOURCE

3.5.1 Power Converter

Figures 34 and 35 show, respectively, a block diagram and a schematic diagram of the power converter. This unit is designed to supply a total of 3 watts. The circuit, consisting of an input filter, a reference supply, a timing oscillator, and a power output stage, comprises a self-regulating converter which combines the functions of inversion, line regulation, rectification, and filtering.

The theory of operation of this circuit can best be described by referring to Figure 36. The bold line indicates the basic power handling portion of the circuit. Transistors Q_1 and Q_2 together are alternately

TABLE XIII. PAM OUTPUT CIRCUIT ERRORS

			% of 5 Volts
Gain Errors			
1	Amplifier number 1		-0.001, -0.004
2	10K to 43K attenuator		+0.20 , -0.20
3	MOSFET series chopper (negligible)		--- , ---
4	Amplifier number 2		-0.001, -0.004
5	Total gain errors	Peak	+0.20 , -0.21
		RMS	0.20
DC Errors			
6	Amplifier number 1 due to Input current differentials		+0.015, -0.015
7	Voltage offsets		+0.10 , -0.10
8	+5R reference voltage		+0.25 , -0.25
9	MOSFET leakage currents		+0.012, +0.001
10	Amplifier number 2 due to Input current differentials		+0.08 , -0.08
11	Voltage offsets		+0.10 , -0.10
12	Total dc errors	Peak	+0.557, -0.544
		RMS	0.29
	Total Errors	Peak	+0.76 , -0.75
		RMS	0.36

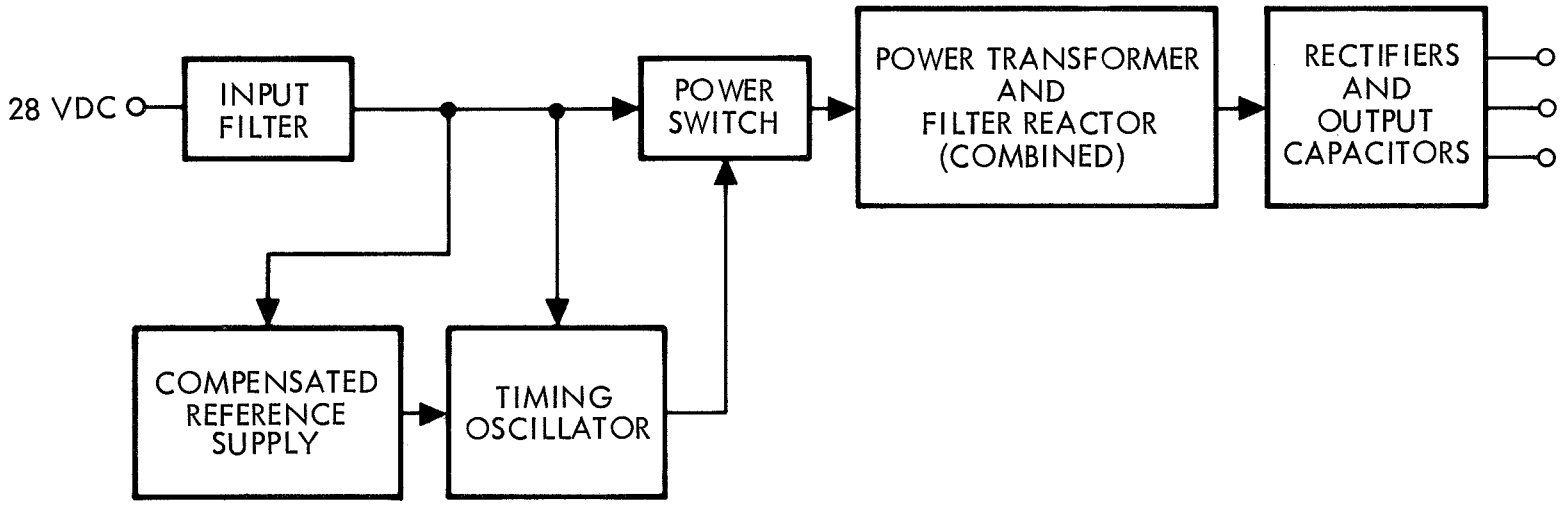


Figure 34. Power Converter MPC-1 Block Diagram

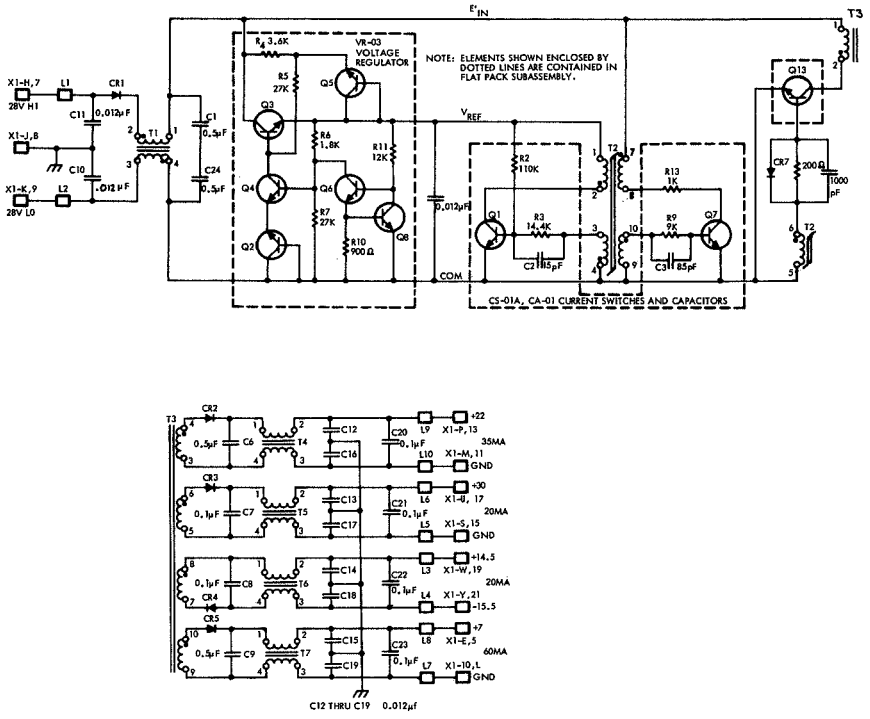


Figure 35. Power Converter MPC-1 Schematic

turned ON for a period of time ΔT_1 and OFF for a period ΔT_2. During ΔT_1, the input (line) voltage is impressed across windings N_p of transformer T_2 and N_1 of saturating transformer T_1. An increment of energy is thereby stored in core T_2. When Q_1 is turned OFF for a period ΔT_2, the current flowing in winding N_p of T_2 is interrupted. The energy stored in the core causes the polarity of the voltage across N_s and N_p suddenly to reverse. The reversed polarity across N_p causes a current flow through diode D_o into capacitor C_o and the load. The rate at which power is delivered to the load is related to the ratio $\Delta T_1/\Delta T_2$ of power switch Q_1; by controlling this ratio, the output voltage, E_o, can be regulated.

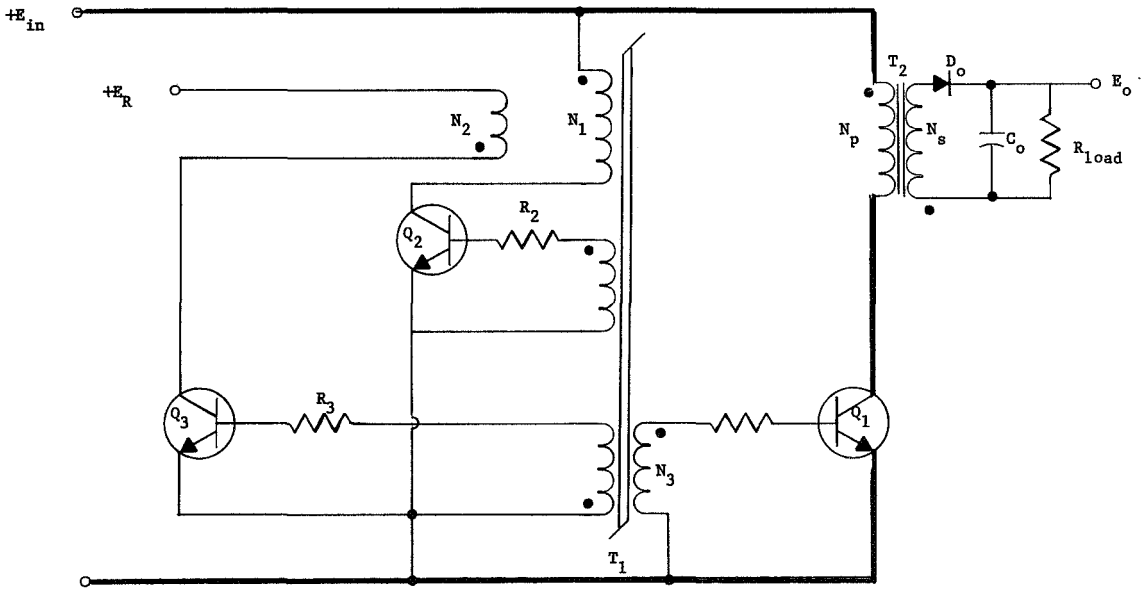


Figure 36. Basic Converter Circuit Schematic

The circuit, consisting of transistors Q_2 and Q_3, transformer T_1, and resistors R_2 and R_3, comprises a standard magnetically-coupled square wave oscillator. The alternate half cycles of oscillation are not necessarily equal. The period ΔT_2, during which Q_3 conducts (and Q_2 and Q_1 are OFF), is determined by a fixed reference voltage, E_R. In this manner the output voltage can, in principle, be made independent of input voltage. This is shown in the following equations which assume ideal circuit components.

For transformer T_1

$$\Delta T_1 = \frac{2\phi_s N_1}{E_{in} \times 10^8} \text{ (where } \phi_s \text{ is saturation flux)} \tag{13}$$

$$\Delta T_2 = \frac{2\phi_s N_2}{E_R \times 10^8} \tag{14}$$

For transformer T_2

$$\Delta T_1 = \frac{\Delta\phi N_p}{E_{in} \times 10^8} \text{ (where } \Delta\phi \text{ is the steady state flux change in } T_2) \tag{15}$$

$$\Delta T_2 = \frac{\Delta\phi N_s}{E_o \ 10^8} \tag{16}$$

Combining these equations yields

$$E_o = \left(\frac{N_1}{N_2}\right)\left(\frac{N_s}{N_p}\right)E_R \quad \text{NOTE: } E_o \text{ is independent of } E_{in}. \tag{17}$$

Thus, as line voltage increases, the ratio $\Delta T_1/\Delta T_2$ changes in such a manner so as to keep the output voltage constant. ΔT_2 is fixed and ΔT_1, which establishes the variable ON time of Q_1, varies directly with input voltage. Switching frequency hence varies, being a minimum at low line.

The circuit shown previously in Figure 35 was designed to operate at approximately 200 kc at low line (22 vdc). The reference voltage, which establishes time ΔT_2, is provided by a low-level series regulator consisting of transistors Q_4 and Q_3, zener references Q_2 and Q_5, and associated resistors. Because of non ideal components which can result in unequal volt-second products applied to cores T_1 and T_2, the regulation characteristic of the basic converter exhibits a small positive increase in the output with increasing input line voltage. One reason is the change in storage time of Q_{13} under varying line conditions. The additional circuitry within the referenced supply, consisting of transistors Q_6 and Q_8 and resistors R_{10} and R_{11}, provides a means of temperature compensation. Adjustment of R_{10} establishes the desired temperature characteristic.

The tuning oscillator which provides the variable drive pulse to power switch Q_{13} is of standard design. A starting resistor, R_2, at the base of Q_1, establishes reliable starting at all temperature conditions. The reference supply and the timing oscillator consist of integrated circuit devices. The timing core is 1/8-mil Permalloy. Because of the required power level of 3 watts, a discrete component transistor is used for the power switch.

The output transformer (and filter reactor) is of the powder Mo-Permalloy type having a permeability of 160. The output rectifiers are blocked during the ON time of $Q_1(\Delta T_1)$. The output capacitors deliver energy to the load during this variable period. During the time ΔT_2, the output transformer delivers energy to the load and recharges the filter capacitors. Ripple voltage is primarily a function of output capacitance and load. Microminiature ceramic capacitors and filter chokes are used for filtering. The rectifier connections shown in Figure 35 provide plus and minus output levels to the transducer and dc amplifier regulator circuits.

The input filter, T_1, C_1, C_{10}, C_{11}, and C_{24}, limit the amount of ripple fed back into the source. T_1 is wound with special resistance wire in order to dampen the filter response at its resonant frequency. Diode CR_1 provides reverse polarity protection for the converter.

Efficiency of the overall unit is about 70 percent at an input of 28 vdc. Converter components are designed and/or rated to sustain a maximum transient input voltage level of 50V. The input filter inductor T_1 is the largest component in the system. Its size is dictated by the transient susceptibility requirements.

Regulation with line voltage and temperature variations ($-35^{\circ}C$ to $+120^{\circ}C$) is less than 10 percent. Output voltage and drift adjustment is accomplished by variation of R_6 and R_{10} in the reference supply. A dissipative regulator follows this circuit and performs additional filtering and regulation functions (see Series Regulators).

Figures 37 and 38 show the physical layout of the Model MPC-1 Converter. Figure 37 shows the converter with the cover attached in isometric form and also the electrical interconnections between the three basic subassemblies. These are the passive components, flat pack assembly, and transformer and diode assembly, as shown in Figure 39. Figure 38 is an overall layout of the converter and shows the physical interconnections between the basic components and the printed circuit board. The printed circuit board is used to perform the majority of interconnections. The printed interconnecting paths are shown as cross-hatched areas on the layout drawing.

Figure 39 is a detailed layout of the flat pack lid assembly located at the top center of the converter package, as shown in Figure 38. It shows the printed circuit board with the assembled transformer T_2. T_2 is the timing transformer used in the magnetically coupled square wave oscillator. Mounted on top of T_2 are two discrete ceramic capacitors, C_4 and C_5, and resistor R_{14} and diode CR_7. CR, R_{14}, and CR_7 are wired in parallel to form the base drive circuit for the power output transistor Q_{13}.

Figure 40 shows a top view of the 3/8 x 3/8 inch flat pack used to mount the active components of the converter. It contains output transistor Q_{13} and three integrated circuit chips. The first chip, CS-01A, consists of transistors and resistors used to make up the current switch portion of the converter. The second chip, CA-01, consists of MOS-type capacitors C_2 and C_3. The third chip, VR-03, is the voltage regulator used to supply V_{REF} to the current switch transistor Q_1. The black lines shown interconnecting the three integrated circuit chips and power transistor Q_{13} are gold wires. The collector of Q_{13} is connected directly to an isolated pad inside the package, as shown by the drawing. Note that the other three chips all use a common mounting pad. This pad is connected to the COM connection of the flat pack, pins 1 and 2.

Figures 41 and 42, respectively, show the electrical schematic and integrated circuit assembly of the Voltage Regulator VR03. Dimensions on the sides of the physical layout indicate overall size in thousandths of an inch. As per the discussion on voltage regulator adjustment, resistors R_6, R_{10}, R_{11}, R_7, R_5, and R_4 are made adjustable by either blowing out the normally shorted fuse links, or shorting out the normally open links by applying a ball bond over the specially made pad areas.

Figures 43 and 44, respectively, show the electrical schematic and physical layout of the Converter Switch CA-01A. Resistors R_2, R_3, R_9, and R_{13} are made adjustable over a range of ±10 percent. This is accomplished by either blowing out the normally shorted fuse links or shorting out the normally open links, in the same manner as mentioned for the VR03 circuit. Note that although transistors Q_{12}, Q_{14}, Q_{15}, and Q_{16}, and resistor R_{12} are on the chip, they are not used in the converter circuit design.

The following photographs are included:

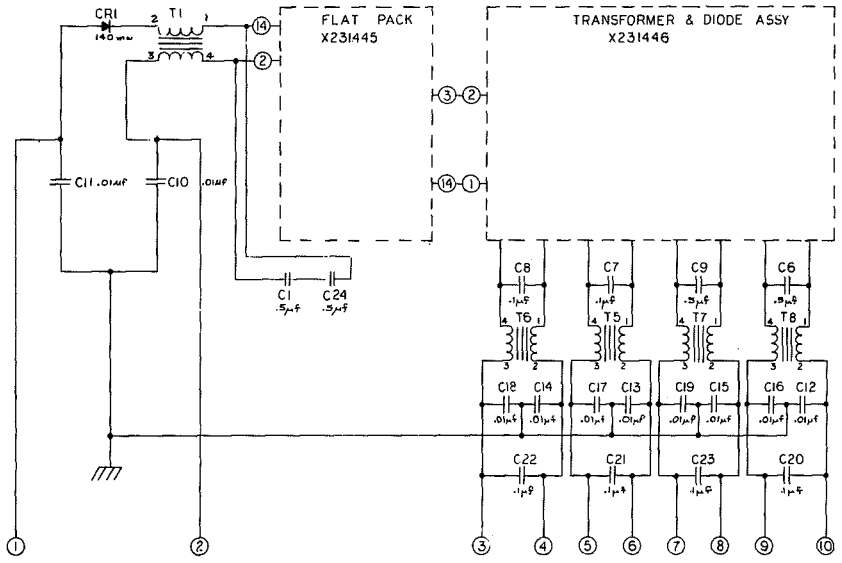
Figure 45. Overall Package

Figure 46. Converter Test Board

Figure 47. Filter Subassembly

Figure 48. T_2 Assembly

Figure 49. Integrated Circuit Module



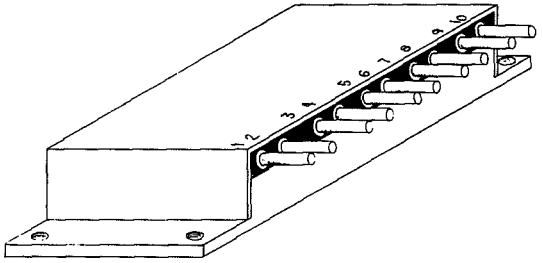


Figure 37. Power Converter Subassembly Drawing

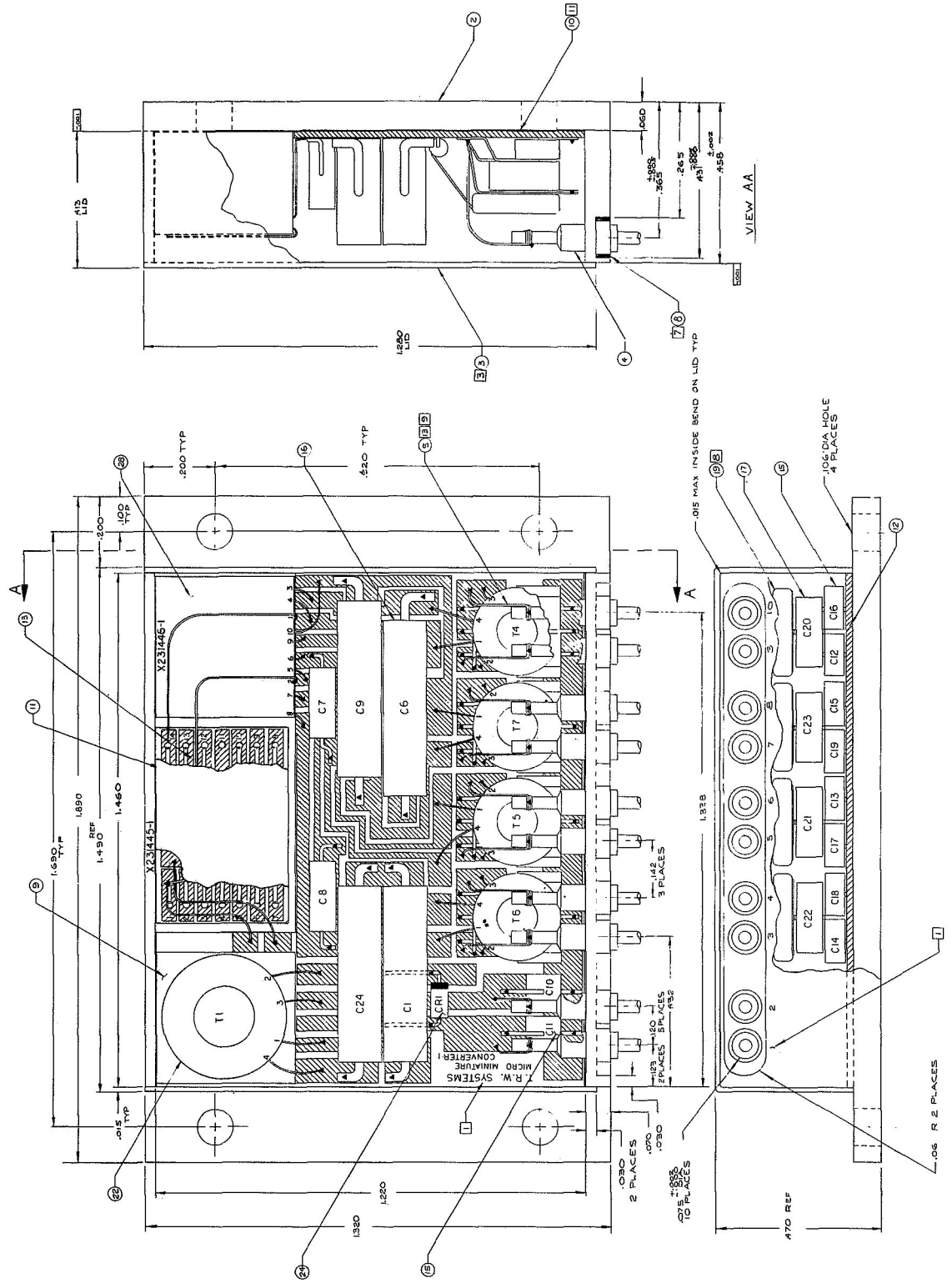


Figure 38. Power Converter Main Assembly Drawing

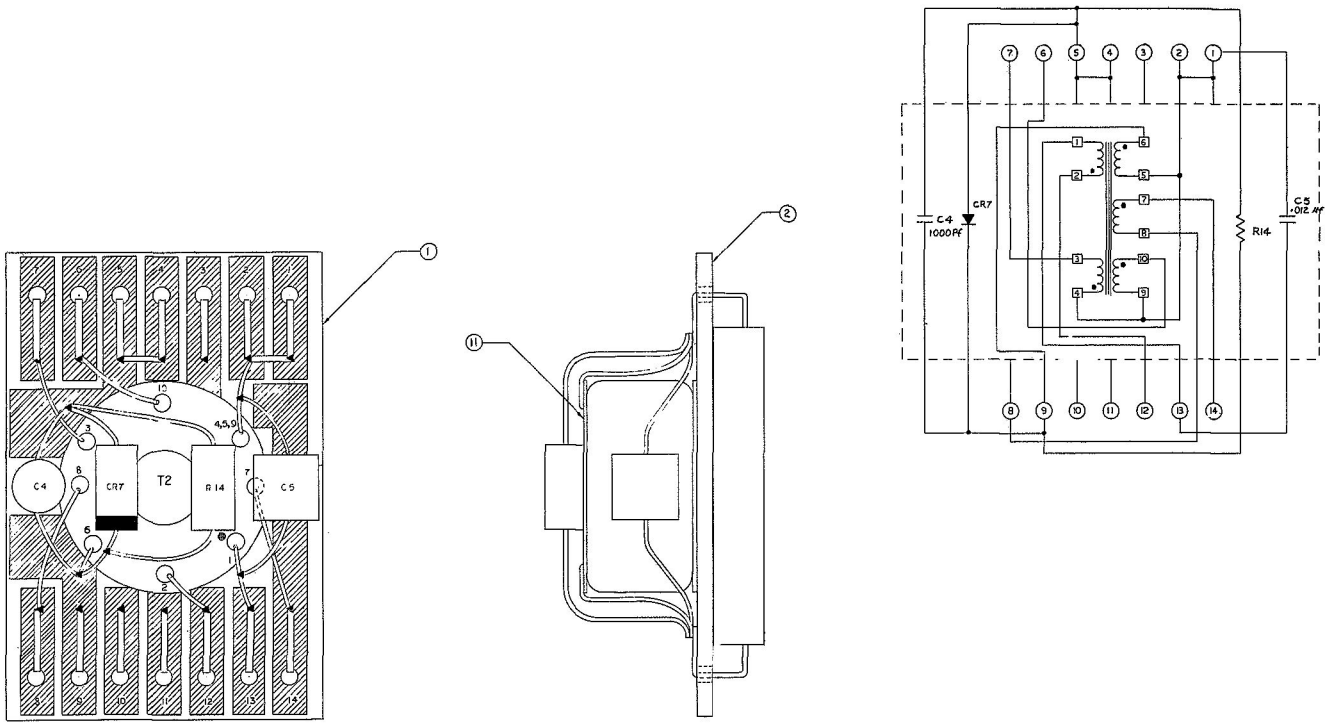


Figure 39. Power Converter Flat Pack Lid Assembly

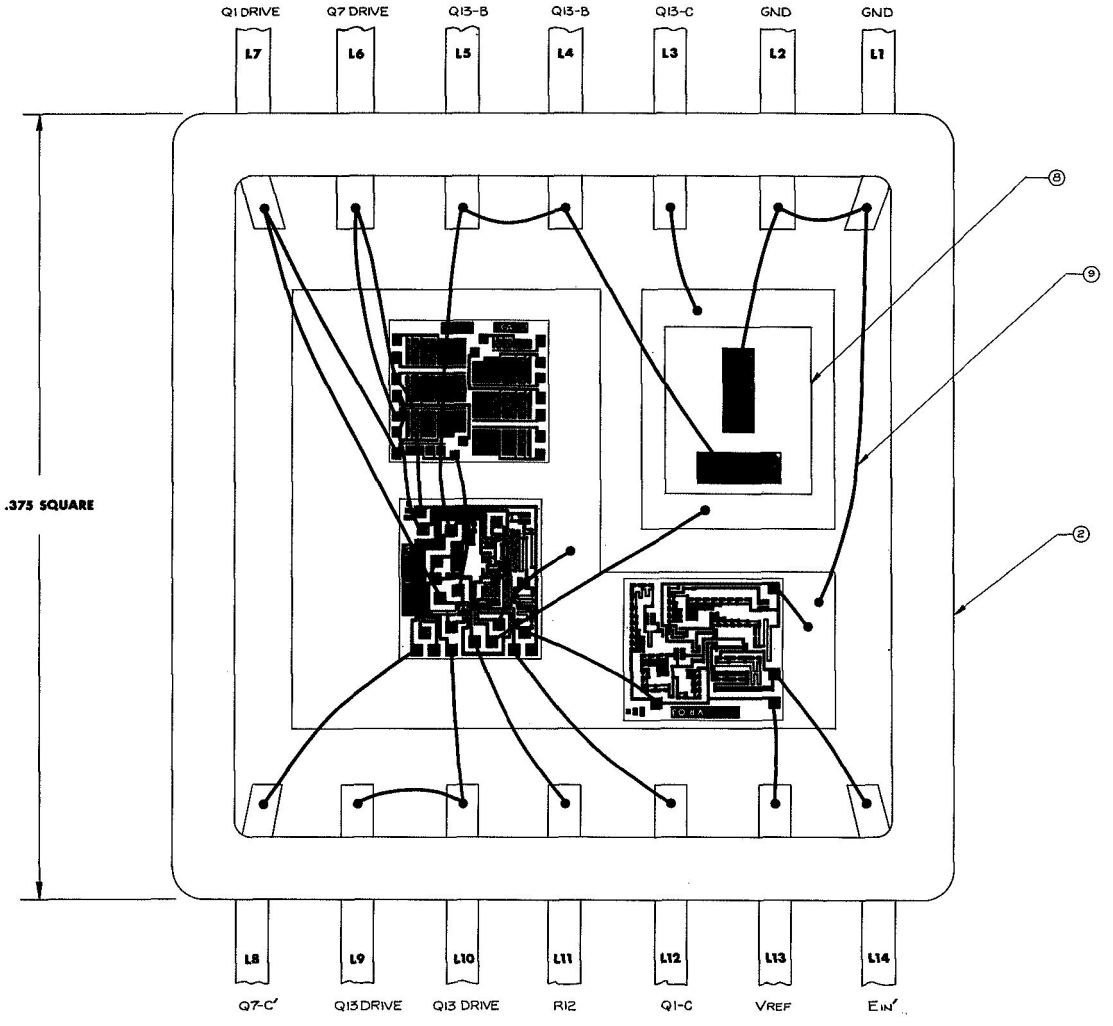


Figure 40. Power Converter Flat Pack Internal Wiring

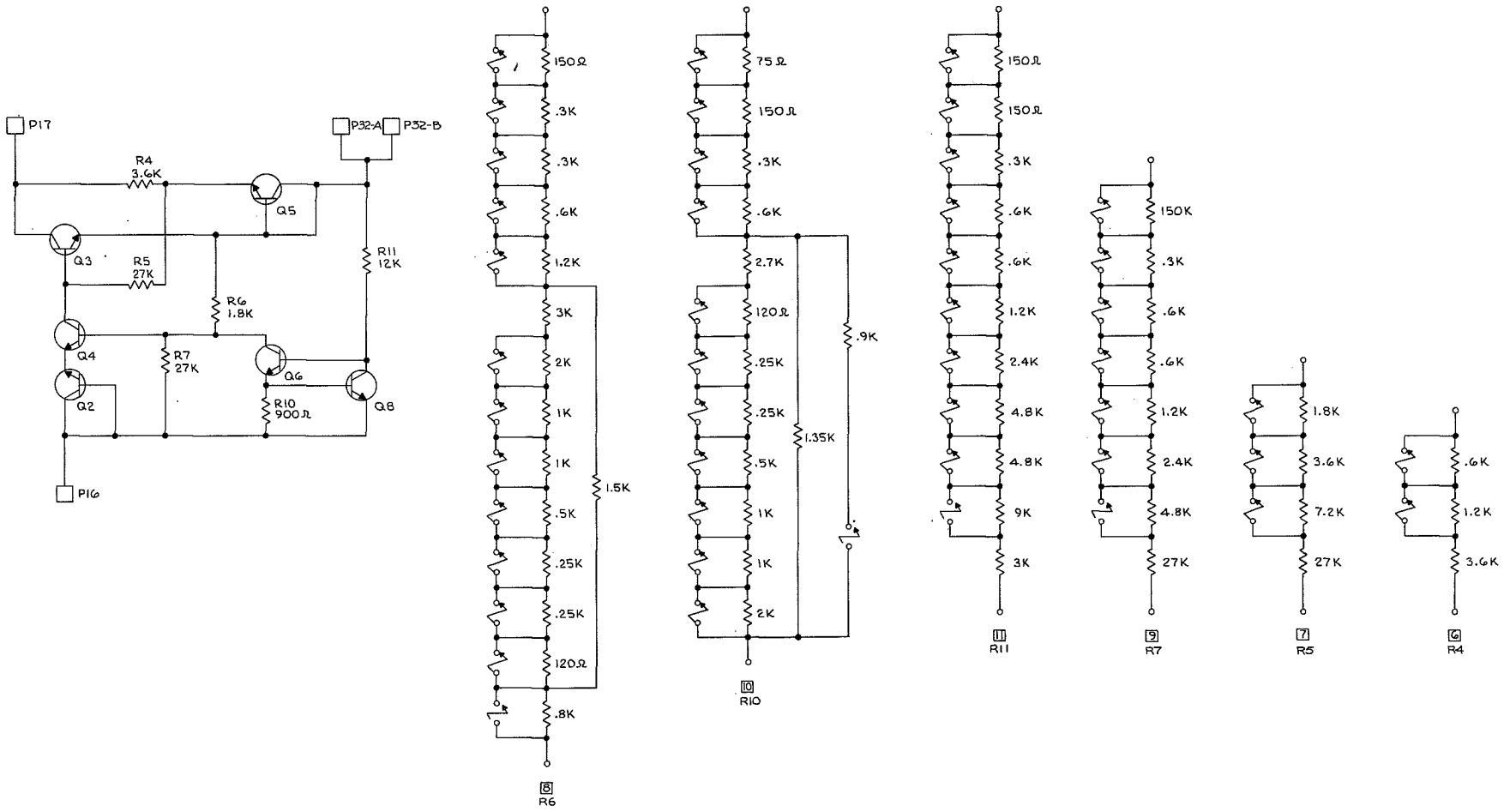


Figure 41. Voltage Regulator (VR03) Schematic

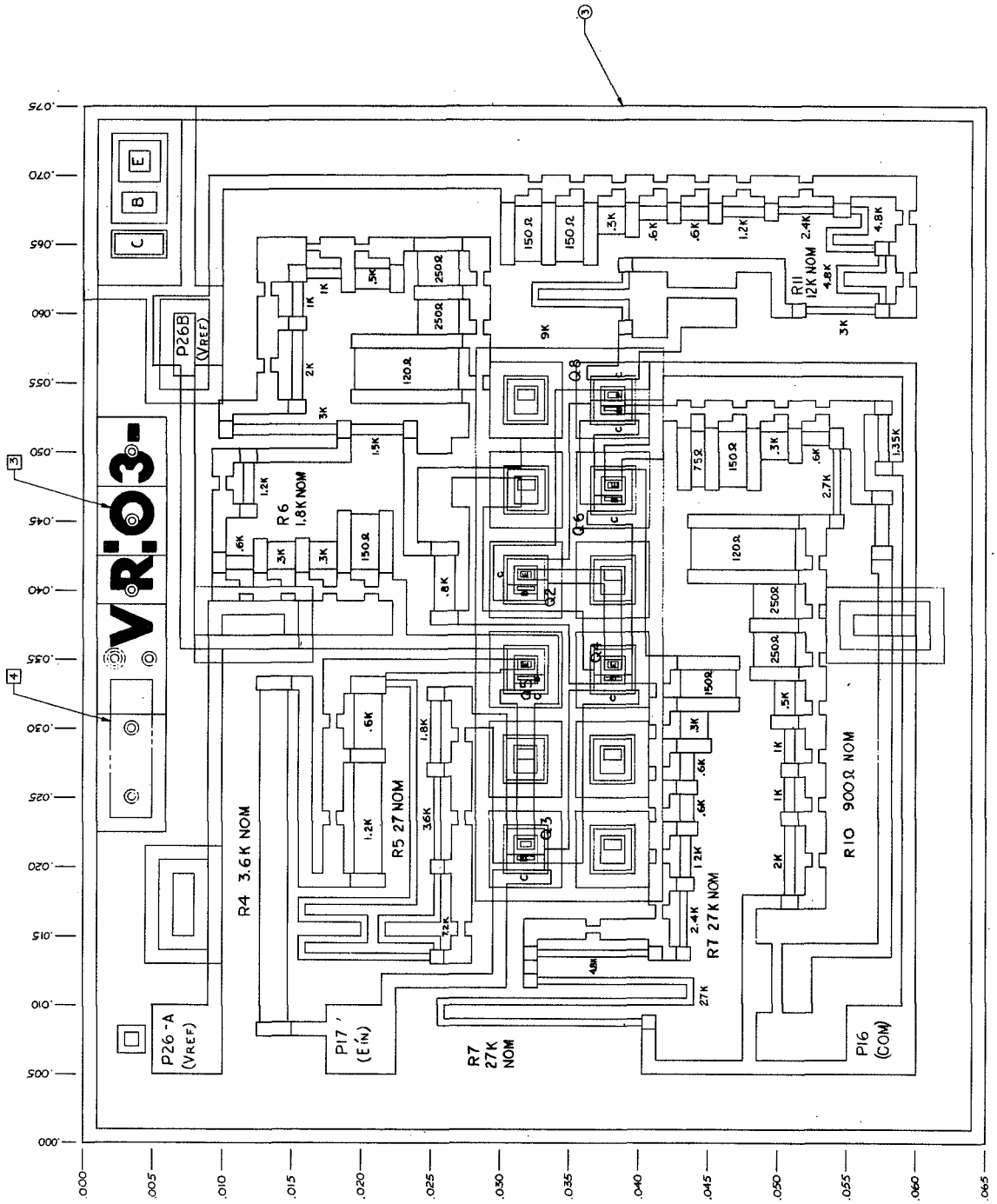


Figure 42. Voltage Regulator (VR03) Assembly Drawing

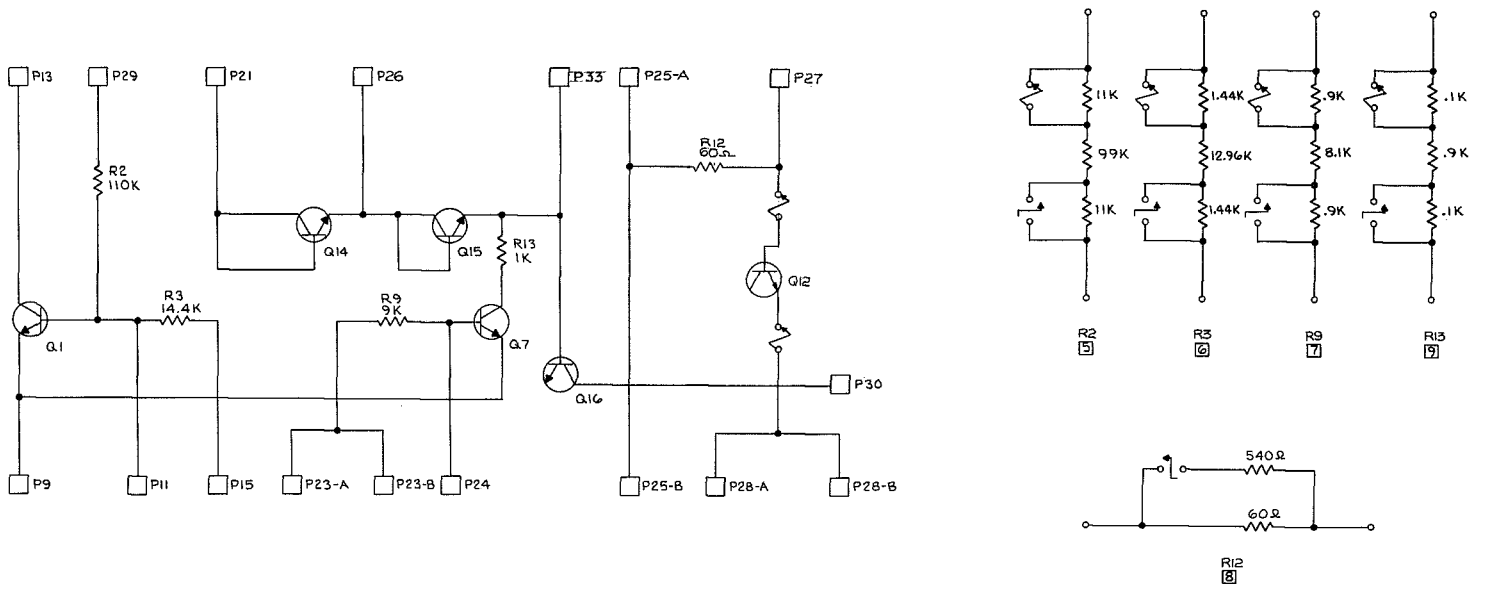


Figure 43. Converter Switch (CSO1A) Schematic

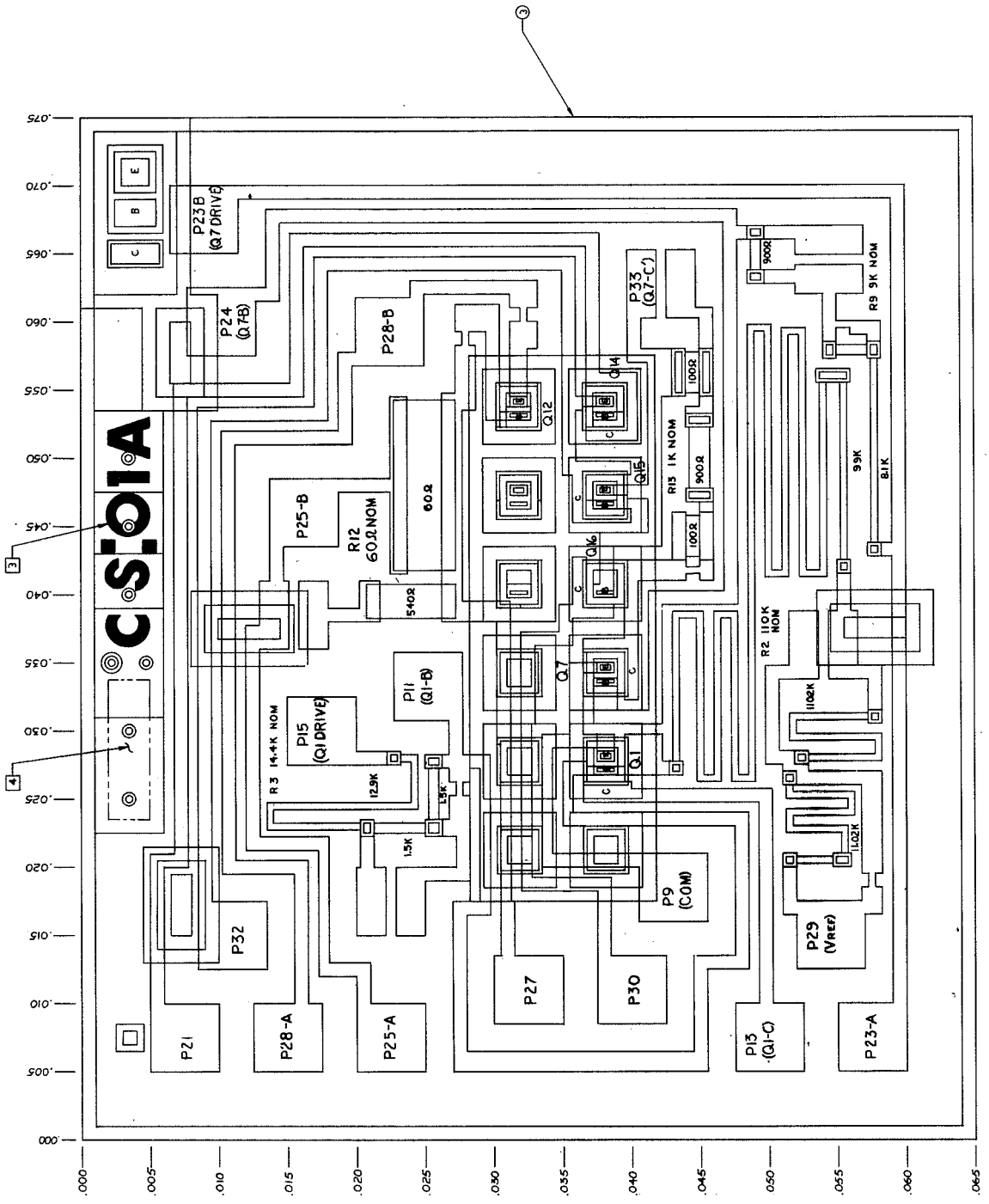


Figure 44. Converter Switch (CSO1A) Assembly Drawing

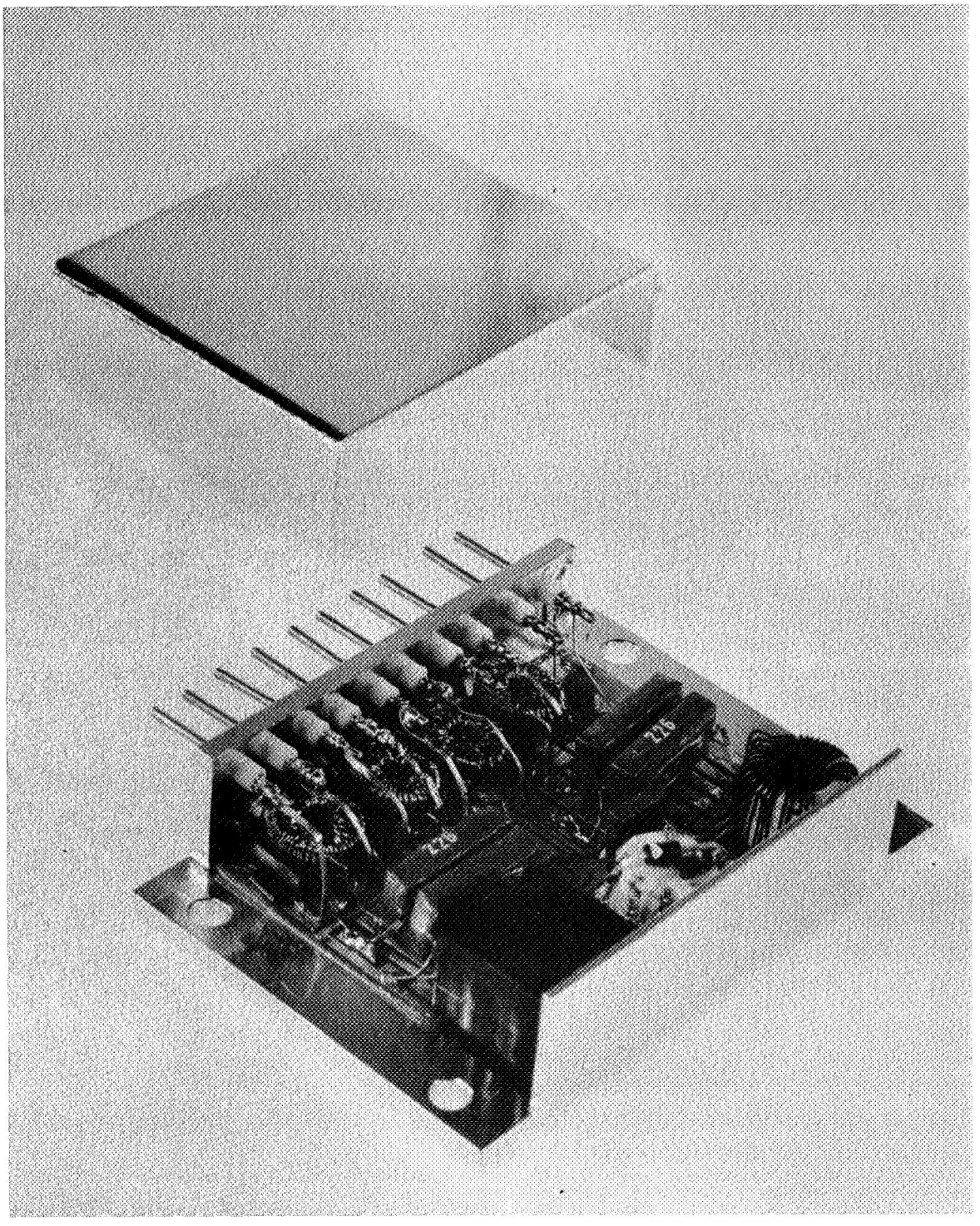


Figure 45. Converter Switch (CSO1A) Overall Package

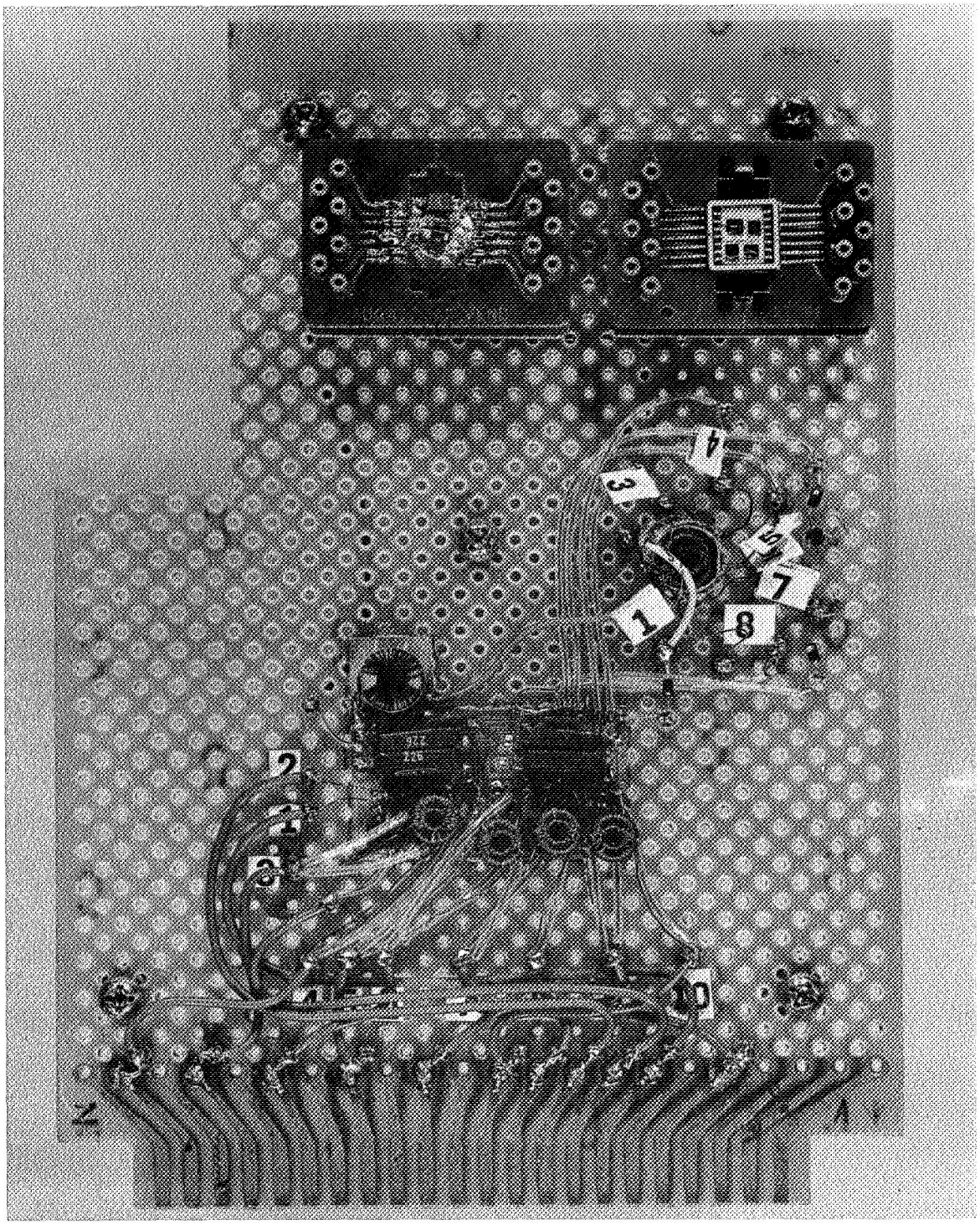


Figure 46. Converter Switch Test Board

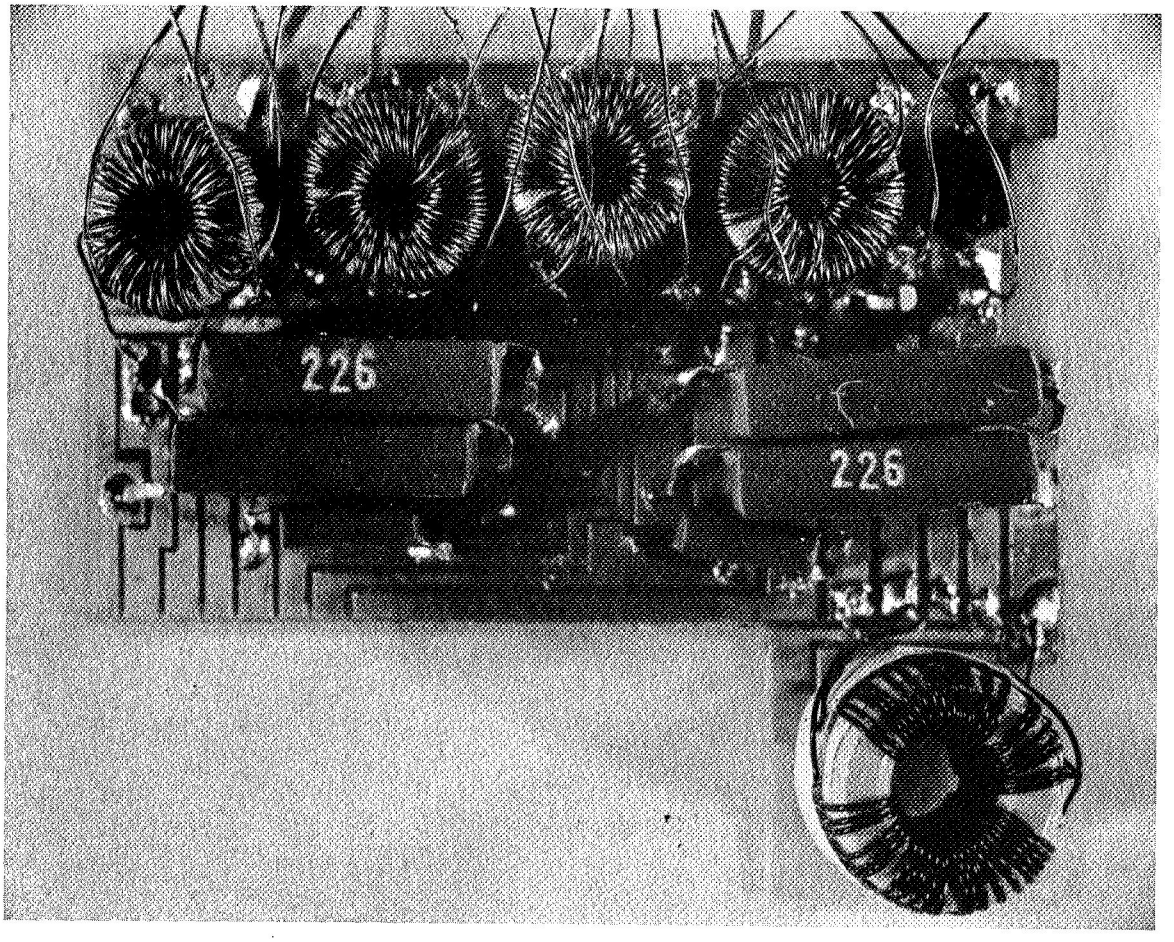


Figure 47. Converter Switch Filter Subassembly

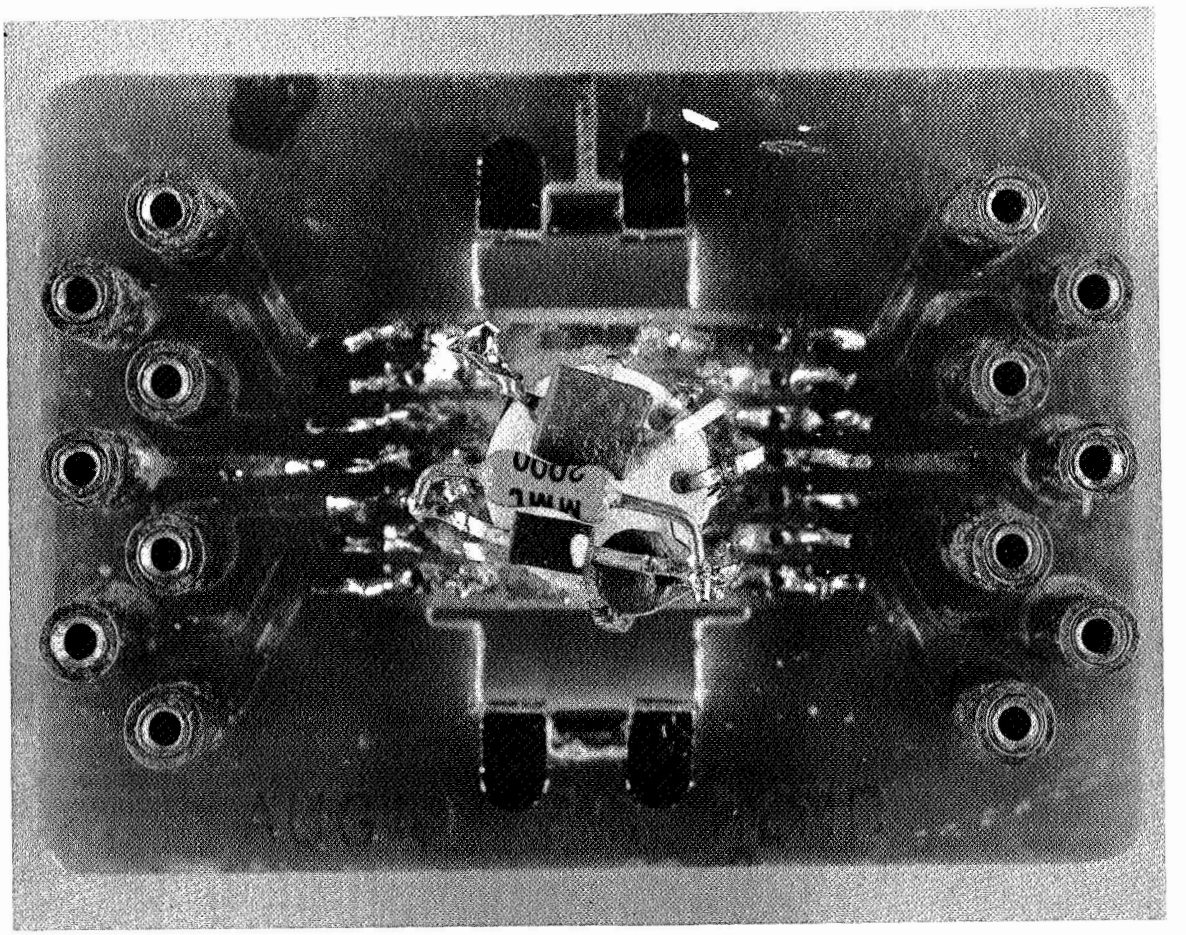


Figure 48. Converter Switch T2 Assembly

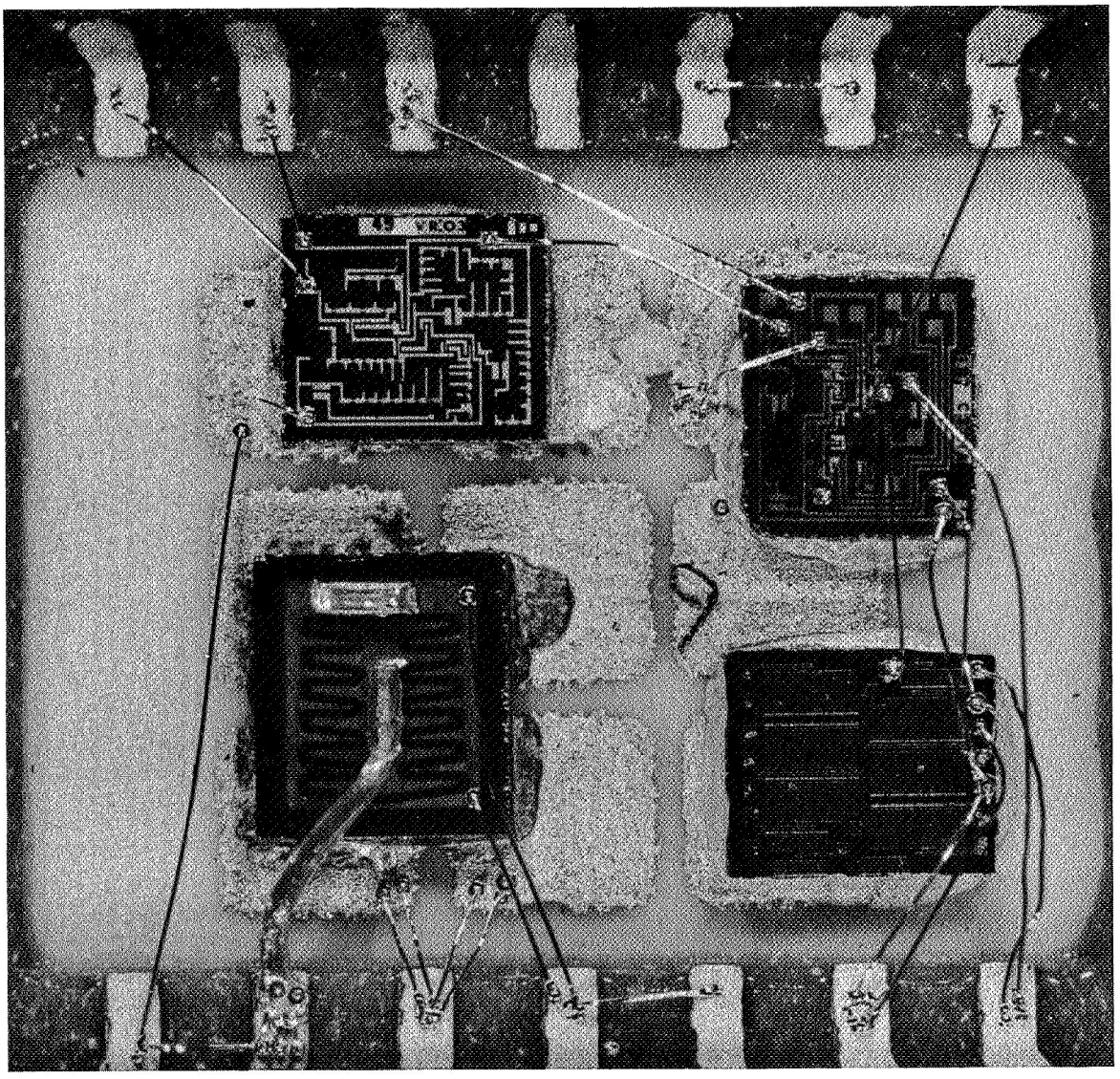


Figure 49. Converter Switch Integrated Circuit Module

A thermal analysis of the converter package is included in Appendix D.

3.5.2 Series Regulators

The TPR16, MPR38 regulators are very similar to the gated regulators, except for the absence of gating circuitry. The LR and RR regulators are essentially different and will therefore be discussed.

Figure 50 is the schematic for these two regulators. Q_2 is a reversed biased diode which stabilizes the voltage which controls the Q_3-Q_4 PNP current generator. This preregulated current generator supplies current into the differential amplifier Q_{12}-Q_{11}. Diodes Q_5 and Q_6 form the voltage reference. Q_{10} is used to supply a temperature dependent current which stabilizes the base voltage of Q_{11} with respect to temperature. This voltage is exactly 5.00 volts. The Q_{11}-Q_{12} differential amplifier establishes the output voltage at 5.00 volts. The output load current is provided by a separate input voltage connection (note V_1 and V_2). This is to minimize power dissipation in the LR ($I_L \simeq 60$ ma) by minimizing the nominal voltage across the regulating transistor Q_7. For the LR application, V_1 is connected directly to the seven-volt converter output, and V_2 is connected to the regulated output of TOR16. For the RR application, both V_1 and V_2 are connected to the regulated output of TPR16.

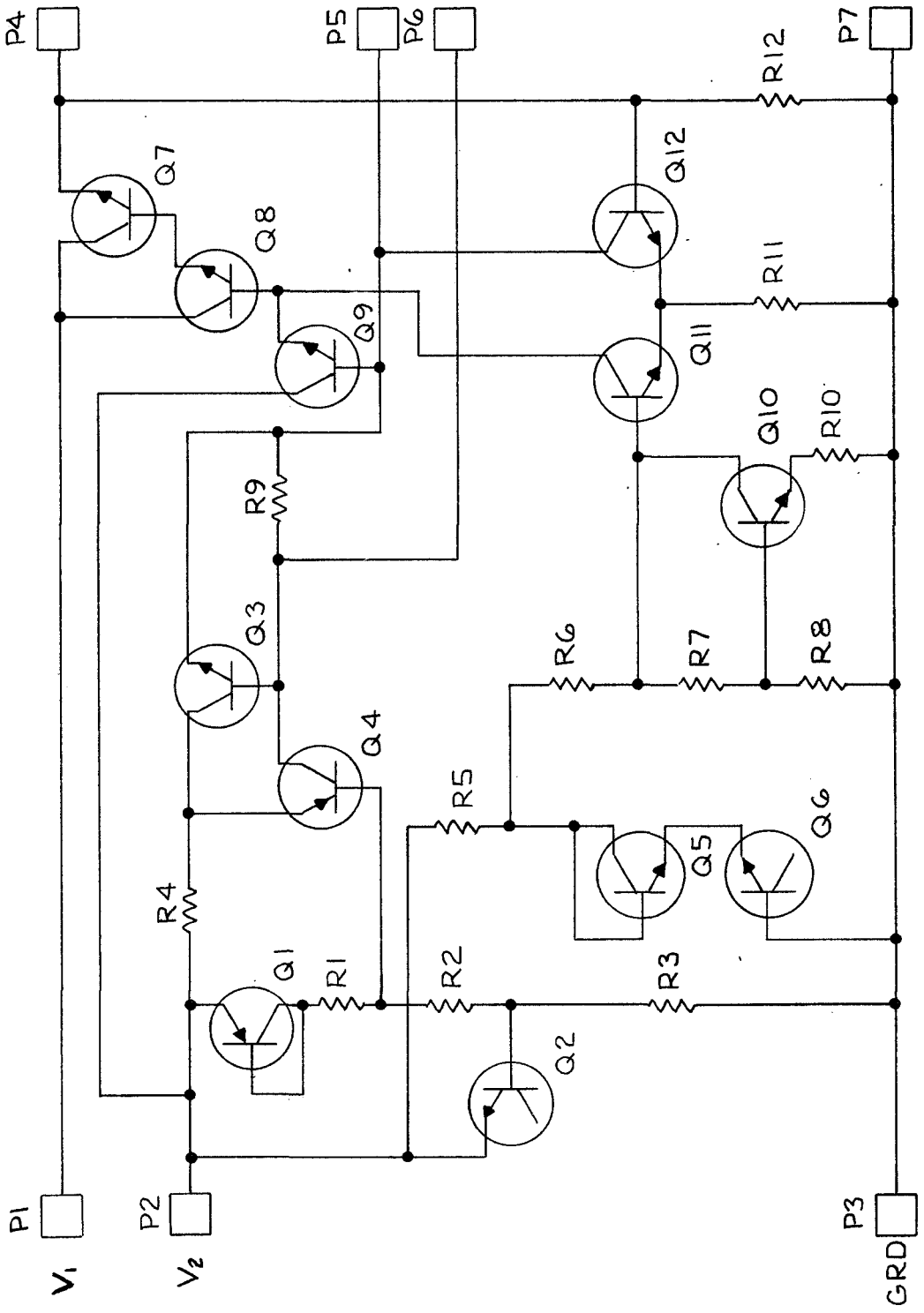


Figure 50. LR and RR Regulator Schematic

4. INTEGRATED CIRCUIT TECHNIQUE

4.1 PROCESSING

Table XIV designates the type of processing used in each of the integrated circuit modules developed by TRW Systems. Items 1 through 7 were developed under Contract No. NAS9-5293, and Items 3 through 7 delivered. Items 8 through 10 were developed and delivered under Contract No. NAS9-4640. Note that the remaining logic circuits are standard Fairchild modules. The PAM output circuit is a combination of discrete components and commercially available amplifiers.

TABLE XIV. PROCESSING TECHNIQUES USED IN TRW INTEGRATED CIRCUIT MODULES

Item	Name		Substrate	BLE	DI	MOS	CR
1	MTR		MCD3		X		X
2	GMR		MCD3		X		X
3	MM-1		MM-1			X	
4	CS01A	Power Converter	MCD1	X			X
5	VR03	Power Converter	MCD1	X			X
6	CA01	Power Converter	CA01			X	
7	LSG05		LSG	X			X
8	SCA41	Signal Modifier	MCD4	X			X
9	SCA42	Signal Modifier	MCD4	X			X
10	CAP	Signal Modifier	CA01			X	

where

BLE ≡ Buried Layer Epitaxy
DI ≡ Dielectric Isolation
MOS ≡ Metal-Oxide-Silicon
CR ≡ Cermet (evaporated) Resistors
* ≡ Developed and Delivered Under Contract No. NAS9-4640

4.1.1 Buried Layer Epitaxial Bipolar Transistors

Figure 51 shows a buried layer epitaxial bipolar transistor in cross section.

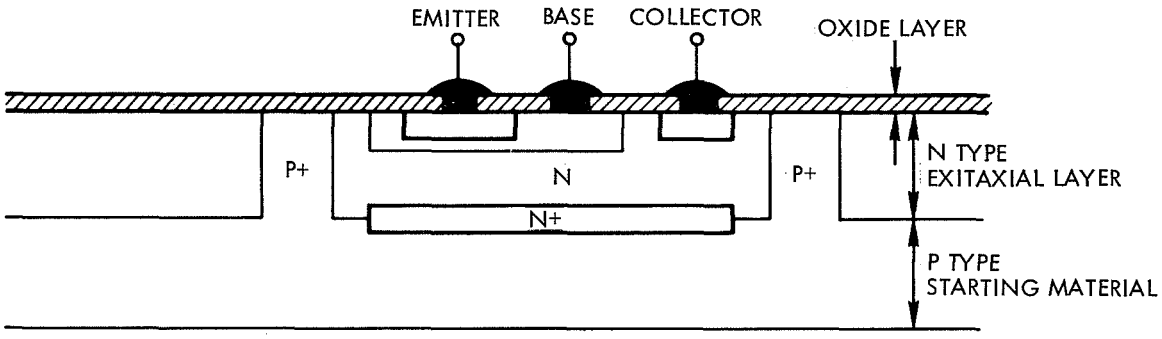


Figure 51. Cross Section of Buried Layer Epitaxial Transistors

The buried layer epitaxial processing technique is standard for TRW Systems and has the following sequence (Note the numerical values given were used in fabricating the MCD1. Different processing was used for the LSG05 and MCD4 substrates):

1.	Starting Material	3.0 ± 5Ωcm P-type <100>
2.	Initial Oxidation	6-1/2F SiO_2 (sodium light; ≈ 13,000 Å thick)
3.	Photoresist Buried Layer N+	(Creates step in surface for post epitaxy identification)
4.	Oxidation	6-1/2F SiO_2
5.	Photoresist Buried Layer N+	(To expose areas for buried layer N+ collector diffusion)
6.	Buried Layer N+ Diffusion	Sb, monitor wafer 3Ωcm P-type sheet resistance 18Ω/□, depth 3.5μ
7.	Epitaxy	0.60 ± 0.15Ωcm; 10 ± 2μ, N-type
8.	Ethyl Silicate Oxide	6 ± 1/2 F SiO_2

9.	Photoresist Isolation Pattern (P+)	To Provide electrical isolated areas
10.	Gate Isolation Diffusion	N-propyl borate, sheet resistance 5Ω/□, depth 15μ
11.	Photoresist Base	To expose base areas
12.	Electrical Isolation Test	To insure electrical isolation, <1μa leakage at 30V
13.	Base Diffusion	B_2O_3, sheet resistance 160Ω/□, depth 3.0μ ≈ 9000 Å SiO_2 grown during diffusion
14.	Photoresist Emitter	To expose emitter areas
15.	Emitter Diffusion	P_2O_5, sheet resistance 3.5Ω/□, depth 1.35 ± 15
16.	Final Oxide	16,000 Å
17.	Photoresist Metal Contact Pattern	To expose electrical contact areas
18.	Base Width Adjustment Diffusion	Adjust for β = 100 ± 20

4.1.2 Dielectric Isolation Bipolar Transistors

Figure 52 shows a dielectrically isolated bipolar transistor in cross section and Figure 53 illustrates the dielectric isolation fabrication steps.

The dielectric isolation technique used to fabricate the MCD3 substrates has the following processing sequence:

1.	Starting Material	0.6 ± 15Ωcm N-type <100> 8 mils thick silicon
2.	Initial Oxidation	6-1/2 fringes SiO_2 (sodium light; ≈ 13,000 Å thick)
3.	Photoresist Isolation	To provide dielectrically isolated areas
4.	Silicon Etch	Etch (2-HF; 15-HNO_3; 5-CH_3COOH) to 25μ depth
5.	Buried Layer N+ Diffusion	Sb, monitor wafer 3Ω cm N-type, sheet resistance 18Ω/□, depth 3.5μ

6.	Dielectric Oxide	16,000 Å
7.	Poly Epitaxial Deposition	Deposit ≈ 6 mils, < 0.01Ωcm N-type, polycrystalline silicon
8.	Parallel Lap	Lap ≈ 1 mil off poly deposit to insure a flat and bump-free surface. Forms mounting surface for Step 9
9.	Isolation Jig Lap and Mechanical Polish	Lap off original substrate to expose islands of single crystal silicon. Final polish 0.1μ alumina
10.	Base Mask Oxide	11,000 Å
11.	Photoresist Base	To expose base areas
12.	Base Deposition	B_2O_3, sheet resistance 180Ω/□, depth 2.5μ
13.	Emitter Mask Oxide	11,000 Å
14.	Photoresist Emitter	To expose emitter areas
15.	Emitter Deposition	P_2O_5, sheet resistance 3.5Ω/□, depth 2.5μ
16.	Final Oxide	16,000 Å
17.	Metal Contact Photoresist	To expose device electrical contact areas
18.	Base Width Adjustment Diffusion	Adjust for beta = 100

Table XV compares dielectrically isolated and buried layer epitaxial integrated circuits.

4.1.3 MOS Transistors

Figure 54 shows an MOS transistor structure in cross section. Note that the oxide layer under the gate electrode is thin (1200 Å) compared with the passivation layer (13,000 Å).

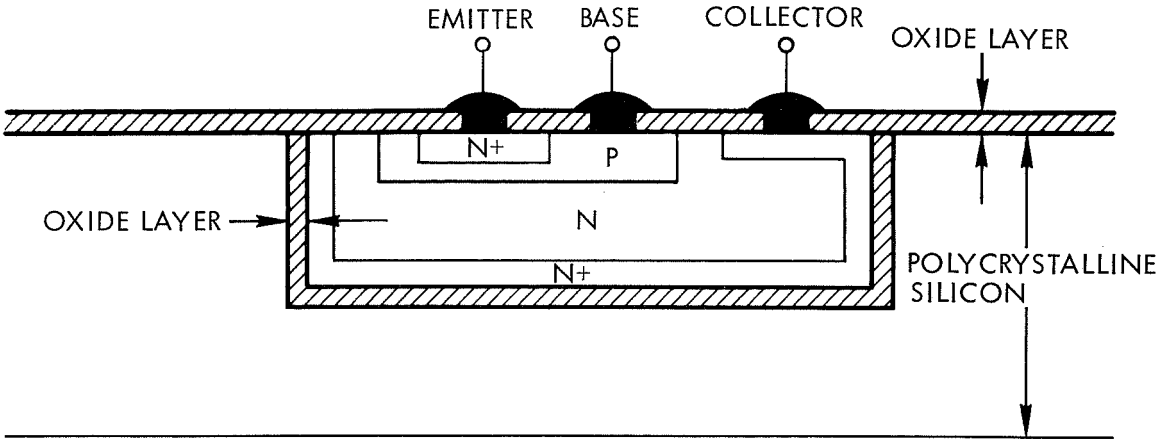


Figure 52. Cross-Section of Dielectrically Isolated Transistor

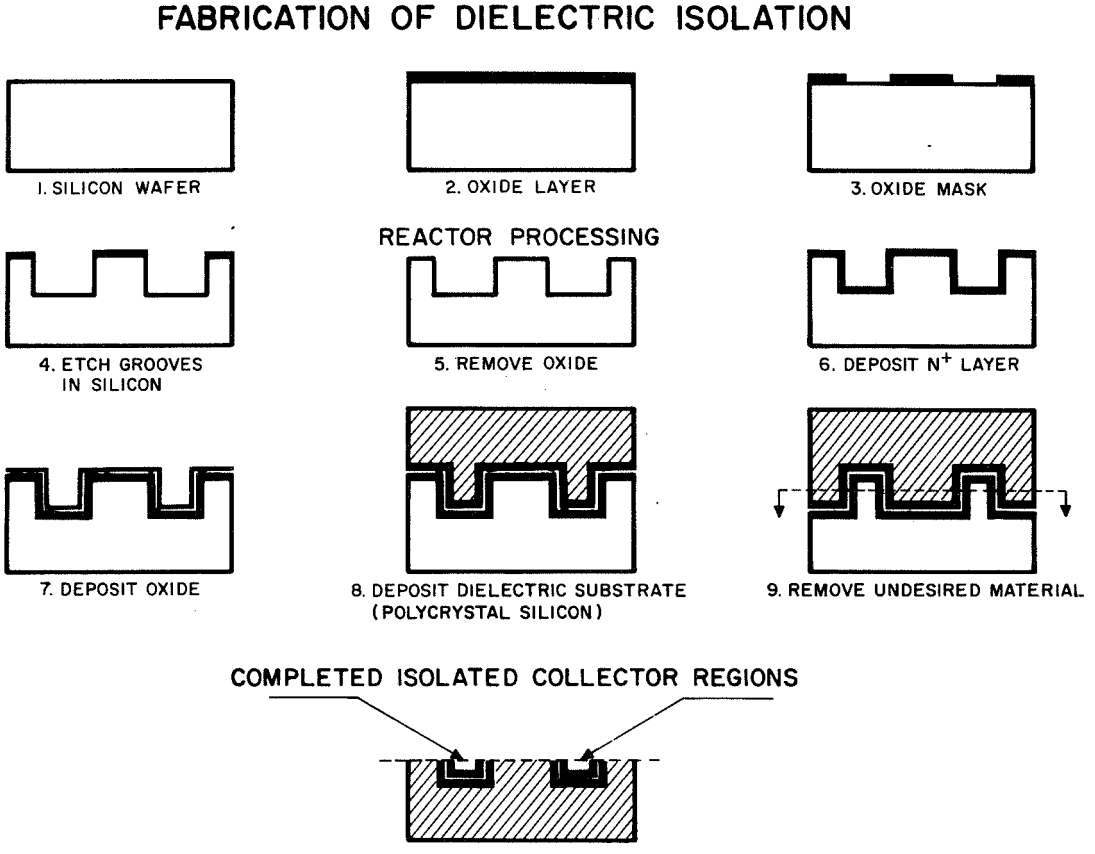


Figure 53. Dielectric Isolation Fabrication Steps

TABLE XV. COMPARISON OF DIELECTRIC ISOLATION WITH CONVENTIONAL CONSTRUCTION

Item	Dielectric Isolation	Buried-Layer Epitaxial
Number of Processing Steps	Few	Many
Potential Yield	High	Moderate
Quality of Semiconductor Active Body	Same as starting wafer	Subject to Epitaxial process variation
Worst Case Impurity	Short, low-temp., shallow junctions	Long, high temp., deep junctions
Thermal Properties	Moderate	Good
Isolation:		
Breakdown Voltage	Unlimited	Limited
Capacitance	Low	High
Space-Charge Field	Low	High
Leakage Current	Low	Moderate
Parasitic Transistor Action with Substrate	Nonexistent	Design problem
Transistor Performance (General)	As good as discrete transistor	Not as good
Transistor Collector Series Resistance	Low	Moderate
General Integral Circuit Compatibility	Good	Good

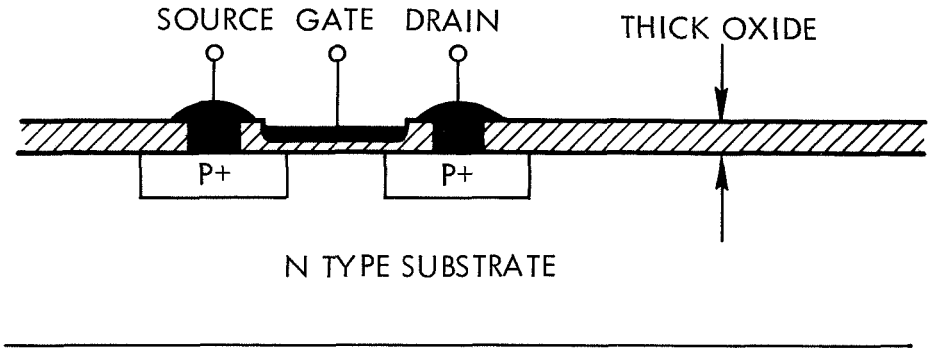


Figure 54. Cross Section of MOS Transistor Structure

The structure is fabricated with the following processing sequence:

1.	Starting Material	3 ohm-cm N-type <111> 8 mils thick silicon
2.	Initial Oxidation	13,000 Å SiO_2
3.	Photoresist Source and Drain	To expose source and drain areas
4.	Source and Drain Impurity Diffusion	P-type, 12 ohm/square 6 microns deep
5.	Photoresist Gate and Contacts	To define gate region
6.	Grow Gate Oxide	1200 Å SiO_2
7.	Photoresist Contacts	To expose silicon at source and drain contacts
8.	Deposit Aluminum Metallization	Electrode and interconnection metallization, 5000 Å of aluminum
9.	Photoresist Metal	Defines electrodes and interconnections
10.	Metal Sinter	Reduces surface oxide at silicon contact regions forming ohmic connections

4.1.4 MOS Capacitors

Figure 55 shows a dielectrically isolated MOS capacitor structure in cross section. Note that the oxide layer over the N+ region is thin (1200 Å) compared with the passivation layer (13,000 Å).

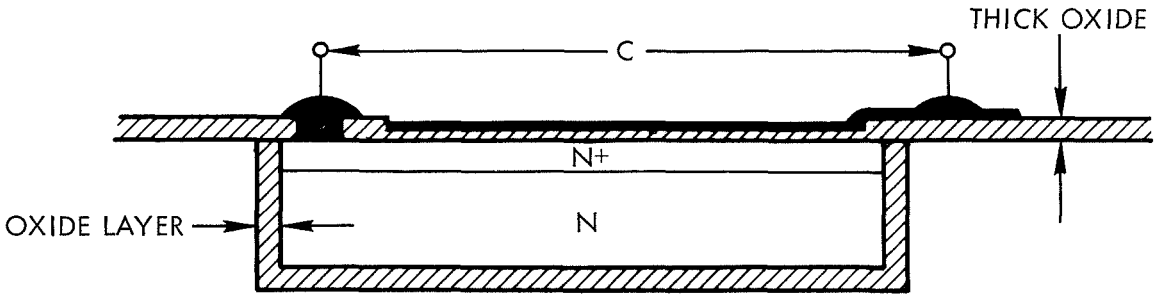


Figure 55. A Cross Section of an MOS Capacitor Structure

The structure is fabricated with the following processing sequence.

1.	Starting Material	0.6 ± 15 ohm-cm N-type <100> 8 mils thick silicon
2.	Initial Oxidation	6-1/2 fringes SiO_2, ≈ 13,000 Å thick
3.	Photoresist Isolation	To provide dielectrically isolated areas
4.	Silicon Etch	Etch (2-HF; 15-HNO_3; 5-CH_3COOH) to 25 microns depth
5.	Buried Layer N+ Diffusion	Antimony, monitor wafer 3 ohm-cm N-type, sheet resistance 18 ohms/sq., depth 3.5 microns
6.	Dielectric Oxide	16,000 Å
7.	Poly Epitaxial Deposition	Deposit ≈ 6 mils, <0.01 ohm-cm N-type, polycrystalline silicon

8.	Parallel Lap	Lap ≈ 1 mil off poly deposit to insure a flat a bump-free surface. Forms mounting surface for Step 9.
9.	Isolation Jig Lap and Mechanical Polish	Lap off original substrate to expose islands of single crystal. Final polish 0.1 micron alumina.
10.	N+ Mask Oxide	11,000 Å
11.	Photoresist	To expose N+ area
12.	N+ Deposition	N-type, 2.5 ohm/square
13.	Photoresist Capacitor and Contacts	Defines capacitor and contact area
14.	Grow SiO_2 Dielectric	1200 Å of SiO_2
15.	Photoresist Contacts	To expose silicon for counter electrode contact.
16.	Deposit Metallization	500 Å titanium and 6000 Å of aluminum
17.	Photoresist Metal	Defines electrodes
18.	Metal Sinter	Forms ohmic contact to N+ silicon for counter electrode

4.1.5 Resistors

Figure 56 shows a thin film evaporated cermet resistor with metallization in cross section. A buried layer epitaxial substrate is assumed. Note the cermet resistor is also used with the MCD3 dielectrically isolated substrate.

The processing sequence which follows includes all of the surface processing used on a monolithic compatible integrated circuit.

The resistors are fabricated as follows: cermet (Cr:SiO) is evaporated over the wafer giving a sheet resistivity of 300 ohms per square. Photoresist is applied and developed to mask the desired resistor areas. The excess cermet (Cr:SiO) is etched away, leaving resistors. These resistors are then connected into the circuit by the metallization step.

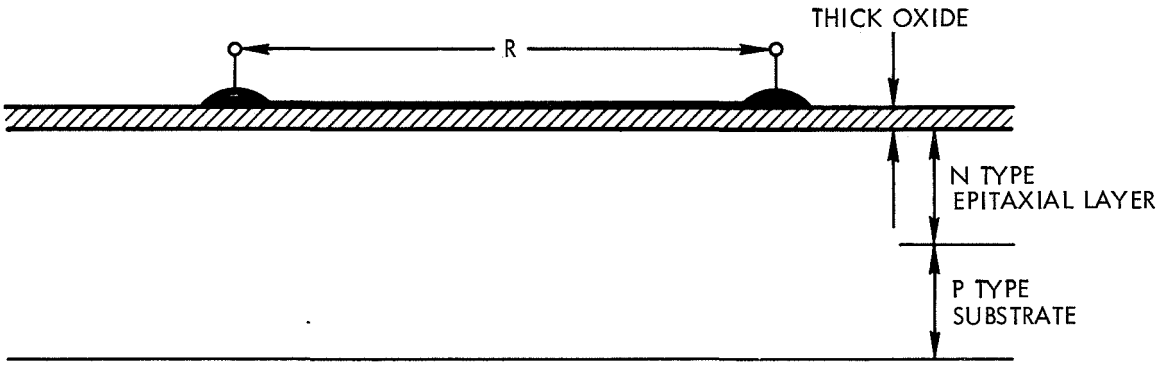


Figure 56. Cross Section of Cermet Resistor

After the substrate (epitaxial or isolated) has been processed and the circuit contact holes etched,

1. Metallizing I	Vacuum deposit 600 Å of titanium and aluminum of 0.02 ohms/square sheet resistance
2. Metallization I Sinter	Heat treatment to insure low resistance ohmic contact to silicon
3. Metallization I Etch	
4. Cermet Deposition	Cr:SiO sheet resistance 300 ± 10 ohm/square, thickness ≈ 300 Å
5. Photoresist Cermet	To leave desired cermet for resistors
6. Metallizing II	Identical to Metallizing I, except for aluminum deposition sheet resistance of 0.04 ± 0.01 ohm/square
7. Photoresist Metallizing II	To leave desired metal for interconnections
8. Metallizing II Sinter	Heat treatment to insure low resistance ohmic contact to cermet
9. Wafer Electrical Function Test	

4.2 DEVICES

The following is a brief description of the integrated devices used in the TRW modules.

4.2.1 MCD1 (see Appendix F)

Figure 57 shows the MCD1 assembly drawing. This substrate is fabricated with the buried layer epitaxial technique. The clear area around the transistor cluster is available for resistors, interconnections, and bonding pads. Crossunders are provided specifically in four locations and generally in any of the transistor positions. A transistor structure can be used as a transistor, diode, capacitor, or crossunder, as determined by the placement of the contact holes in the oxide, aluminum interconnection, and application of the circuit. The CSO1A and VRO3 circuits use this substrate.

Figure 58 shows the transistor lateral geometry in detail. Note that the smallest mask spacing is 0.25 mil.

4.2.2 MCD3 (see Appendix F)

Figure 59 shows the MCD3 assembly drawing. This substrate is fabricated with dielectric isolation to eliminate the dc substrate parasitics associated with the PNP transistors. The GTR and GMR gated regulator circuits use this substrate.

Five types of transistors are included in the MCD3. These are:

a) Low Current NPN. Shown in Figure 60. This transistor is used in all NPN positions except for the regulating element in the positive supply line and the switch in the negative supply line. Nominal h_{FE} of 100 at I_C = 5 ma is typical. This device is also used as forward biased diodes and reversed biased emitter-base diodes (voltage reference).

b) High Current NPN. Shown in Figure 61. This transistor is used as the regulating element in the positive supply line and the switch in the negative supply line. Nominal h_{FE} of 100 at I_C = 60 ma is typical. Collector parasitic bulk resistance, r'_C, is typically less than 15 ohms.

c) Lateral Geometry PNP. Shown in Figure 62. This transistor is used (in a composite configuration) as a constant current generator and as a current monitor for short circuit protection. Nominal h_{FE} of 2 at I_C = 100 μa is typical.

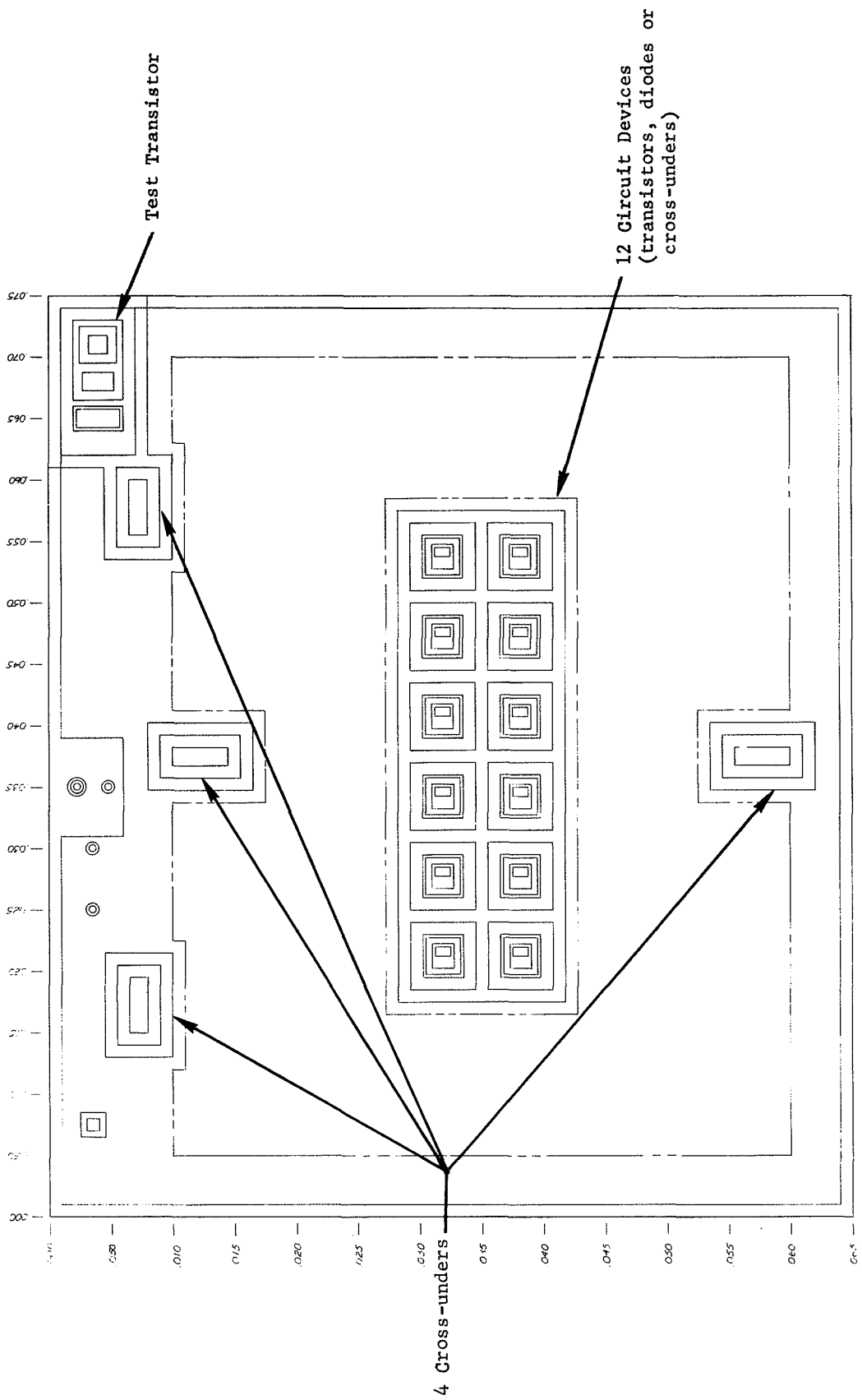


Figure 57. Multi-Circuit Die (MCD1) Assembly Drawing

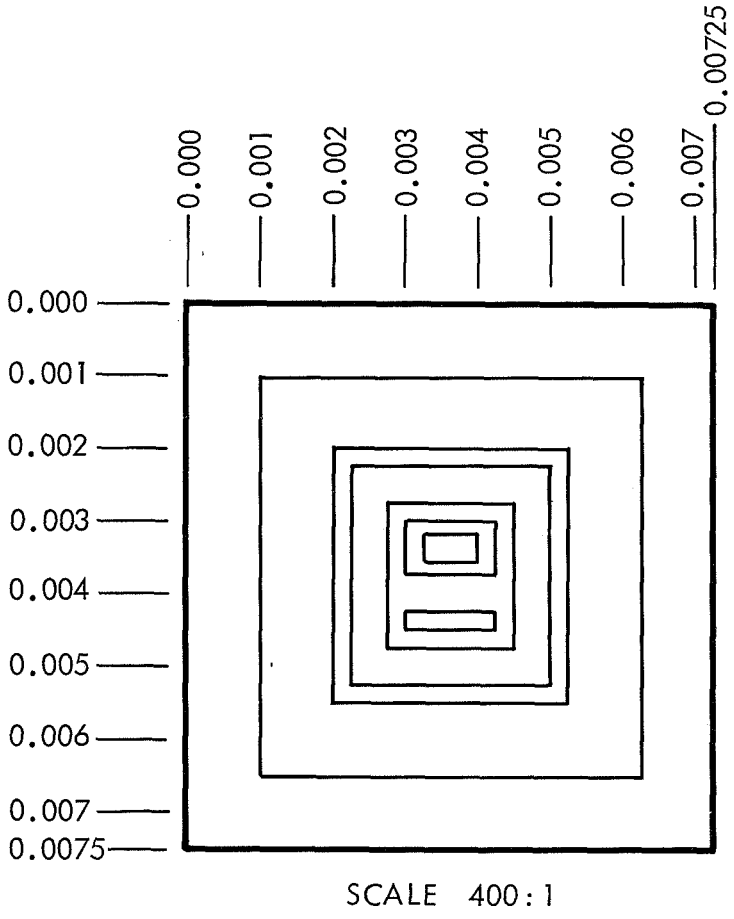


Figure 58. Multi-Circuit Die (MCD1) Transistor Lateral Geometry

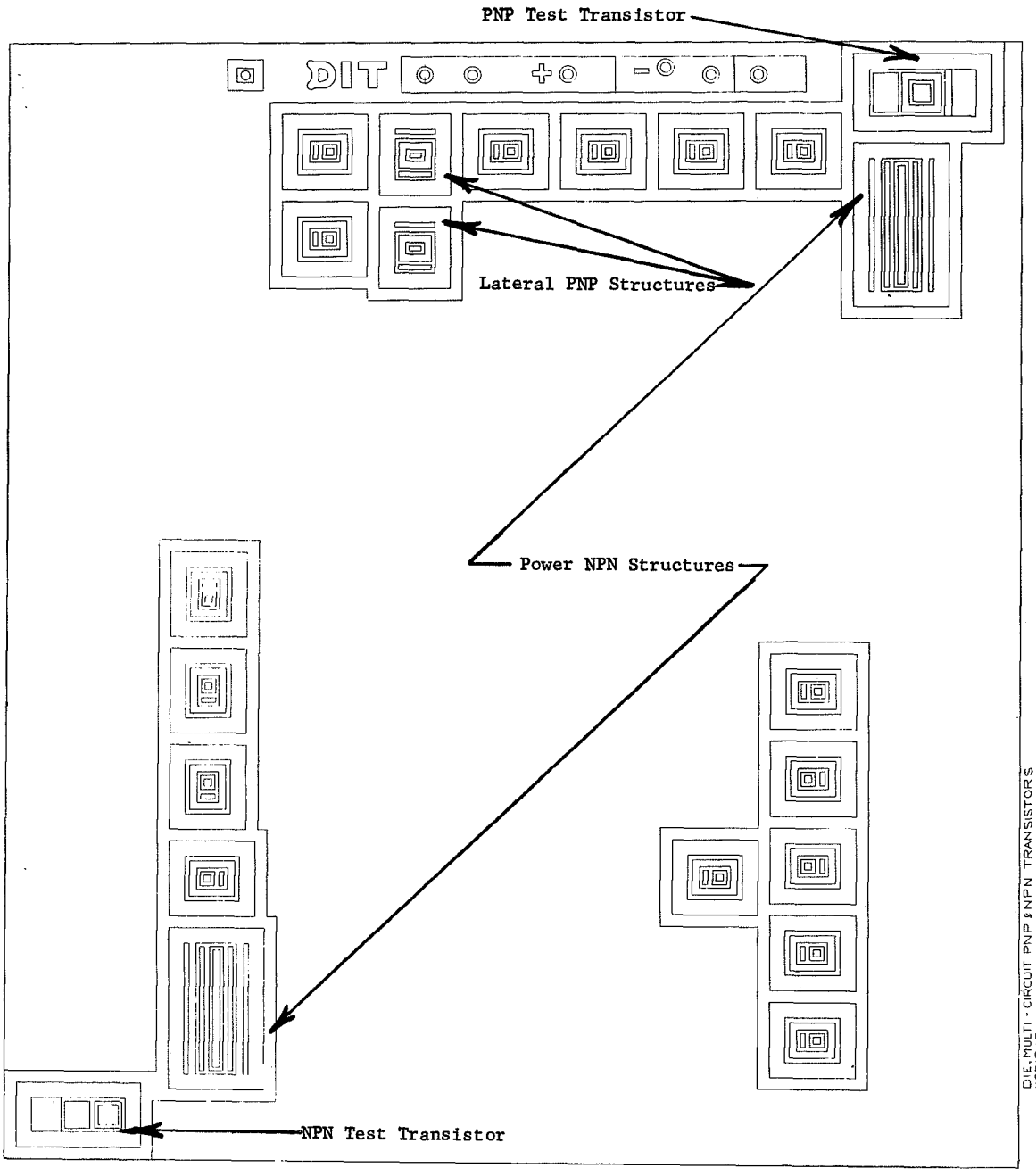


Figure 59. Multi-Circuit Die (MCD3) Assembly Drawing

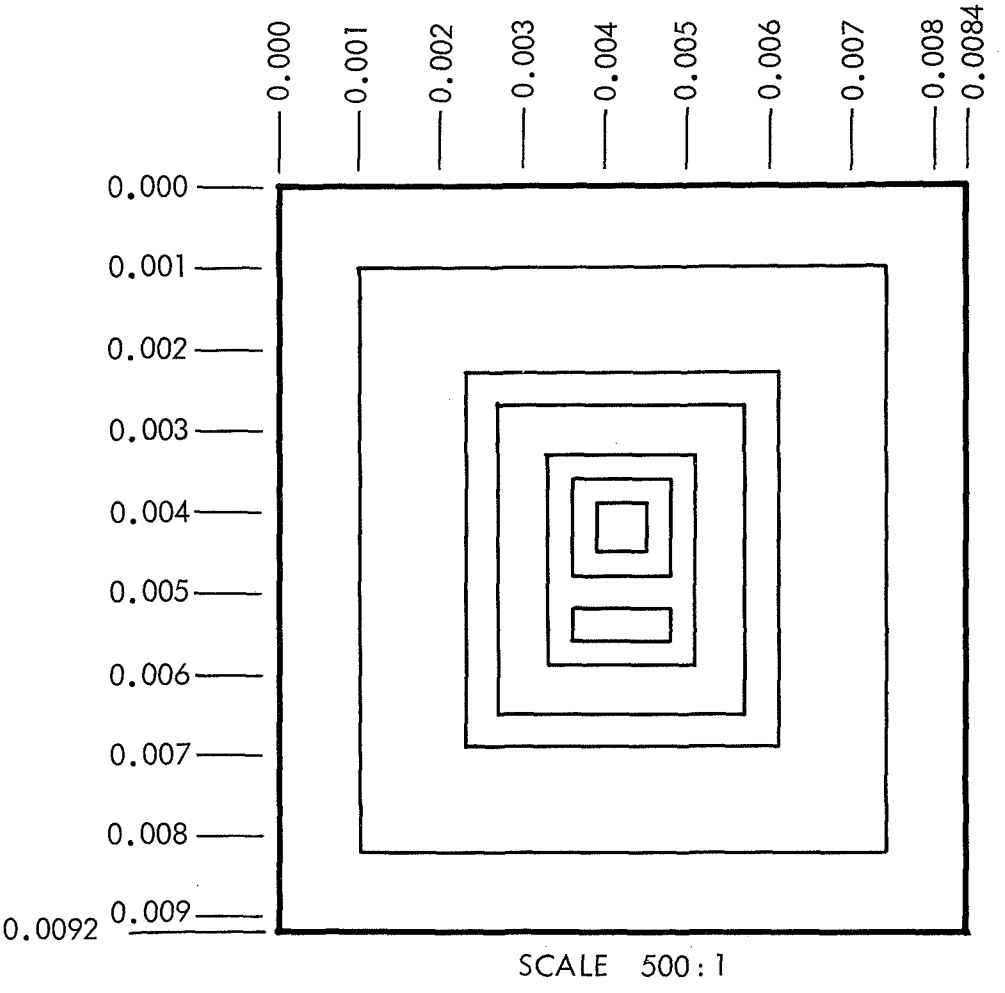


Figure 60. NPN Low Current (MCD3) Transistor Lateral Geometry

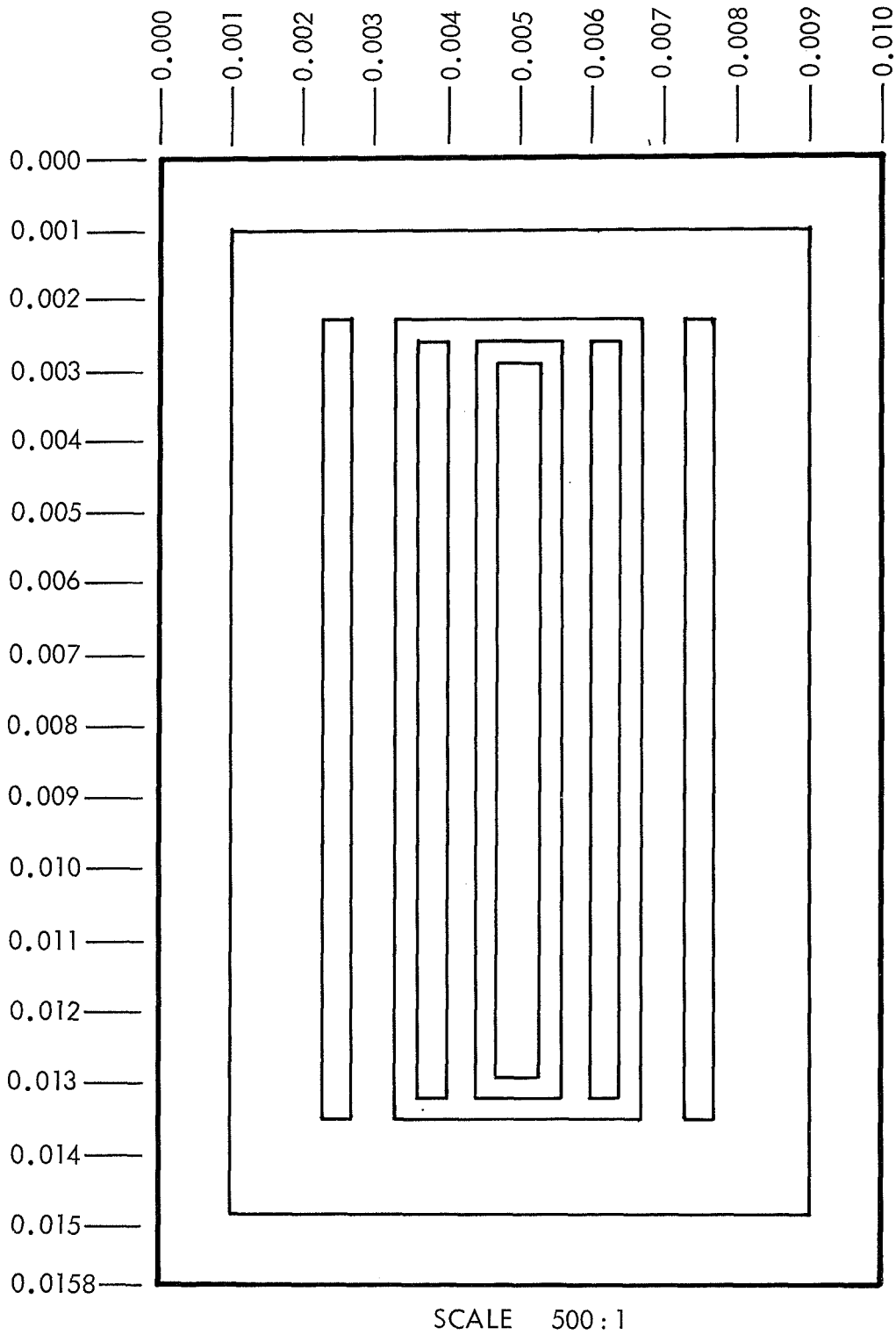


Figure 61. NPN High Current (MCD3) Transistor Lateral Geometry

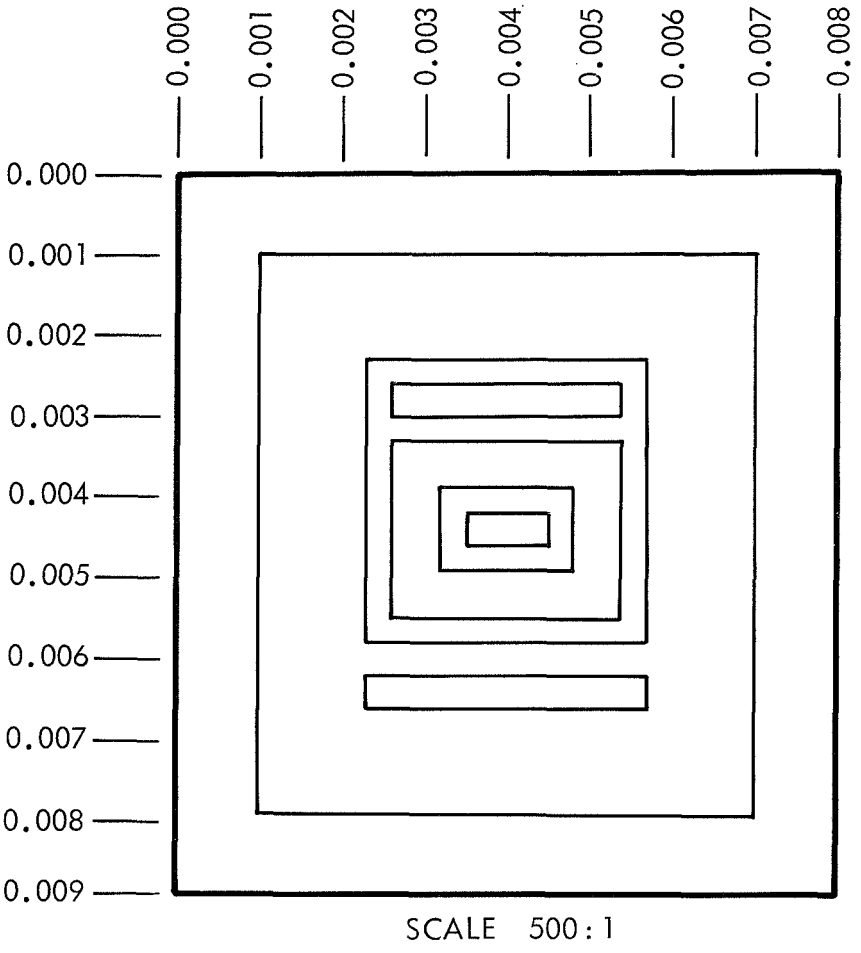


Figure 62. PNP (MCD3) Lateral Geometry

d) NPN Test Transistor. Shown in Figure 63. This transistor is used primarily for device check before metallization.

e) PNP Test Transistor. Shown in Figure 64. This transistor is used primarily for device check before metallization.

Figure 65 shows a special metal transistor test pattern used with the MCD3 substrate.

4.2.3 LSG

Figure 66 shows the substrate used in the LSG05 circuit. Figure 67 shows an enlarged view of the transistor clusters, with Figures 68 and 69 illustrating the individual device lateral geometries.

4.2.4 MM1

The device lateral geometry of the MM1 MOS transistor is shown in Figure 70.

4.2.5 CA01

The CA01 is shown in Figure 71. Eight separate capacitors are available. The six large sections are approximately 50 pf each. The two small sections are 14 pf each. Fuses in the metal interconnect can be blown out to lower the capacitance values. Each of the eight capacitors has subsections weighted in a binary ratio of 8:4:2:1. See Section 4.2.6 about the description of the fuse-adjustment technique.

4.2.6 Resistors

Resistors 1K ohms or larger are ≥ 0.6 mil wide and exhibit the following characteristics:

Absolute Tolerance	±20%
Relative Tolerance (on wafer)	±10%
Ratio Tolerance (adjacent resistors)	±1%
Ratio Tolerance (nonadjacent resistors)	±2.5%
Maximum Absolute Temperature Coefficient	200 ppm/°C
Maximum Tracking Temperature Coefficient	10 ppm/°C

Figure 72 shows the geometry of a typical resistor adjustment fuse link. Probes are placed on the metal interconnect and current is passed

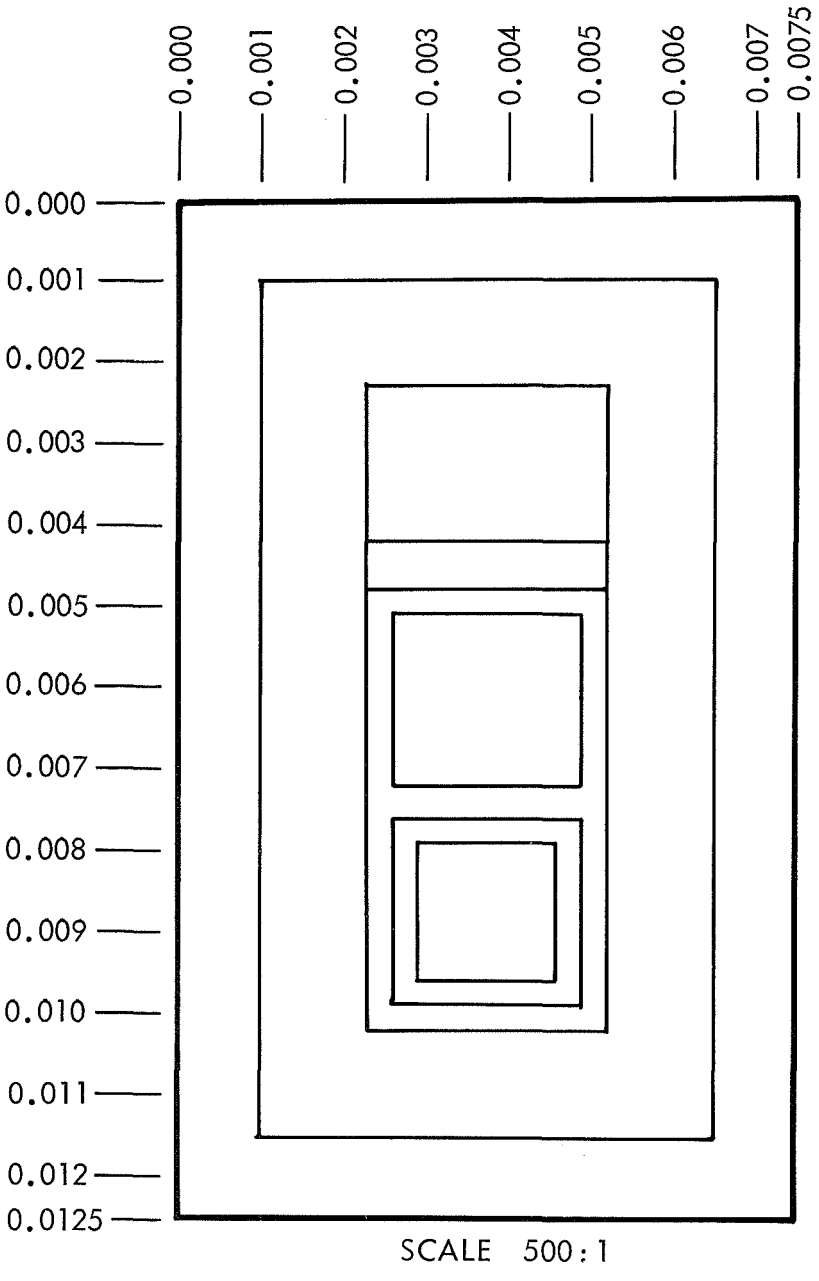


Figure 63. NPN (MCD3) Test Transistor

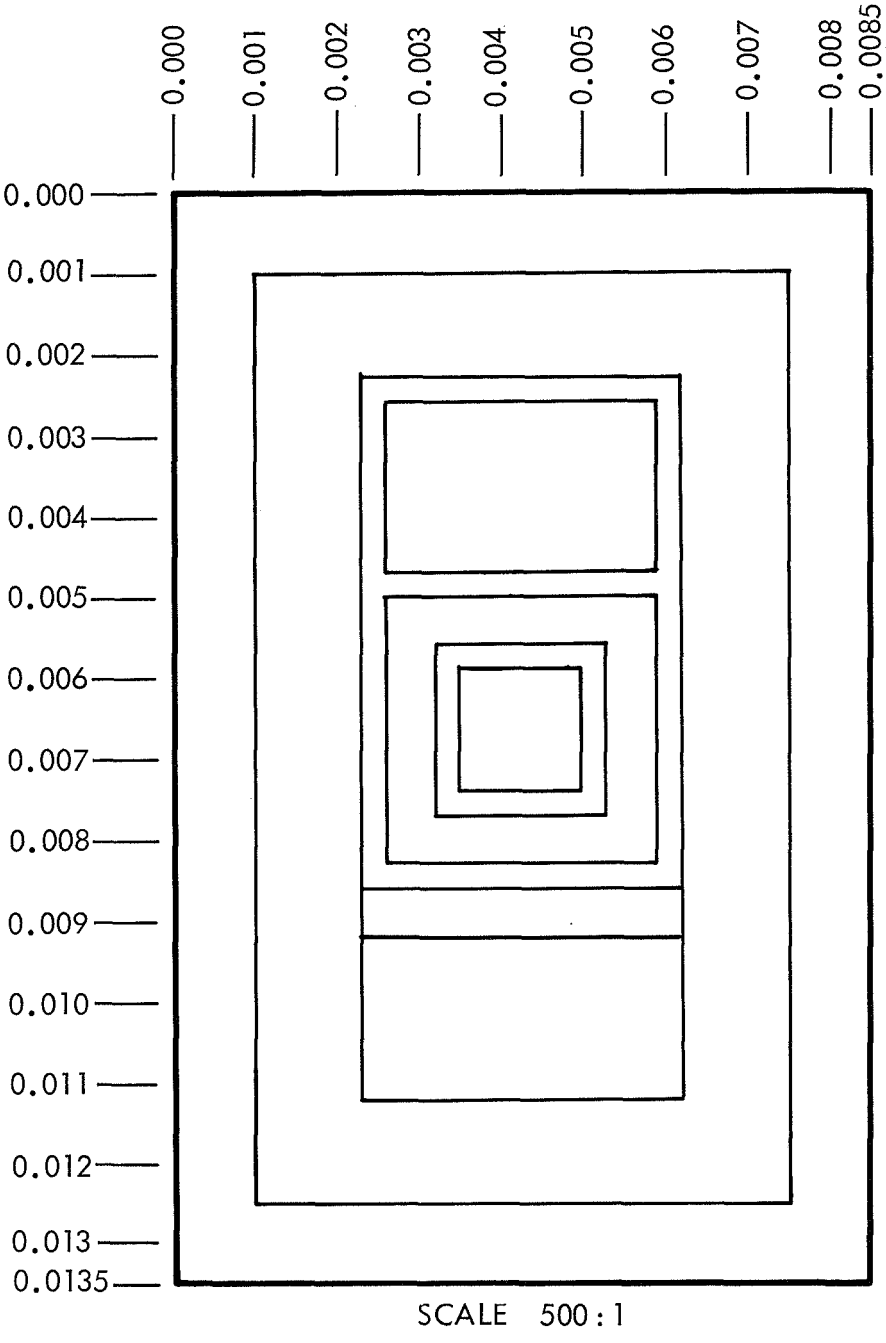


Figure 64. PNP (MCD3) Test Transistor

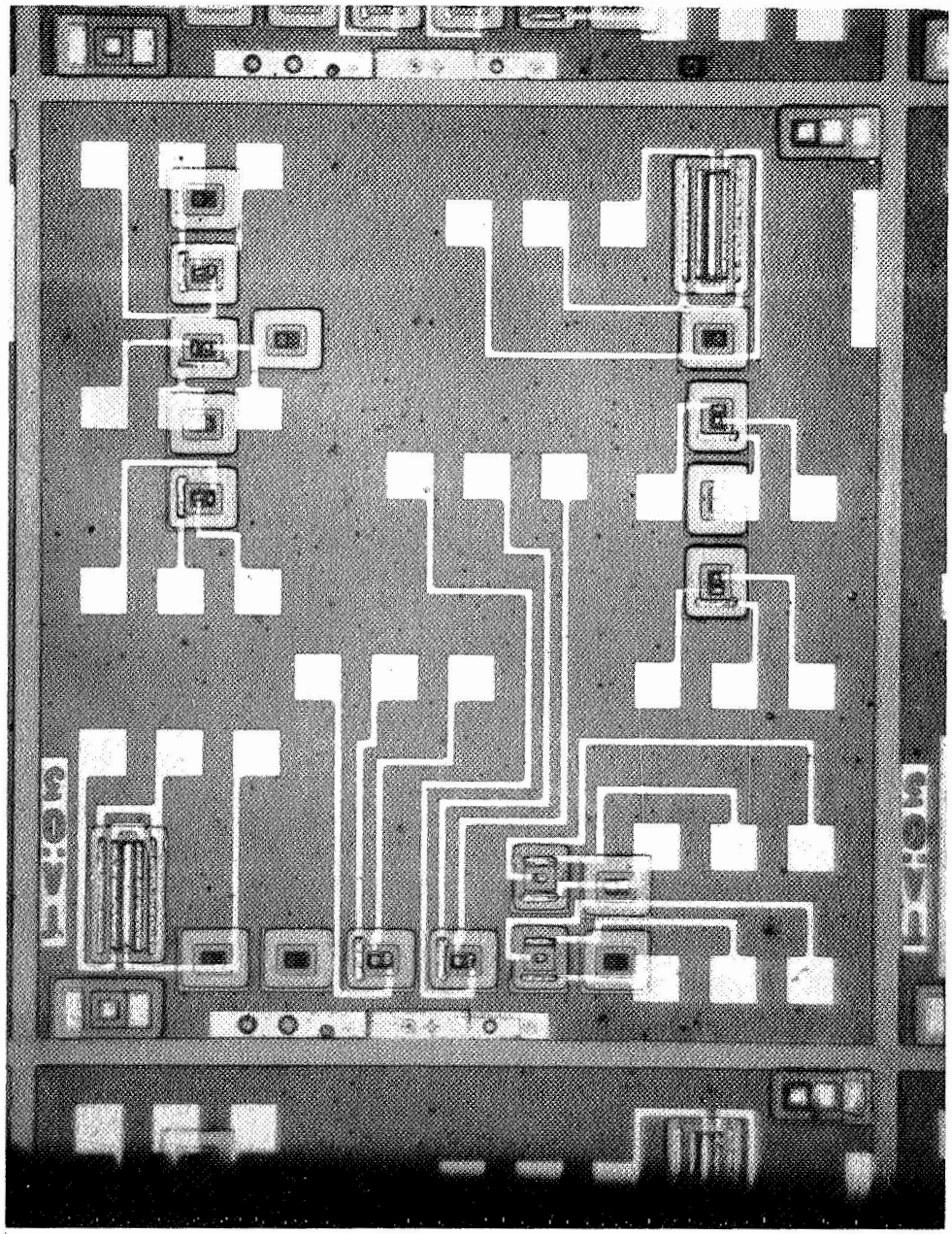


Figure 65. Photograph of MCD3 with TAO3 Test Pattern

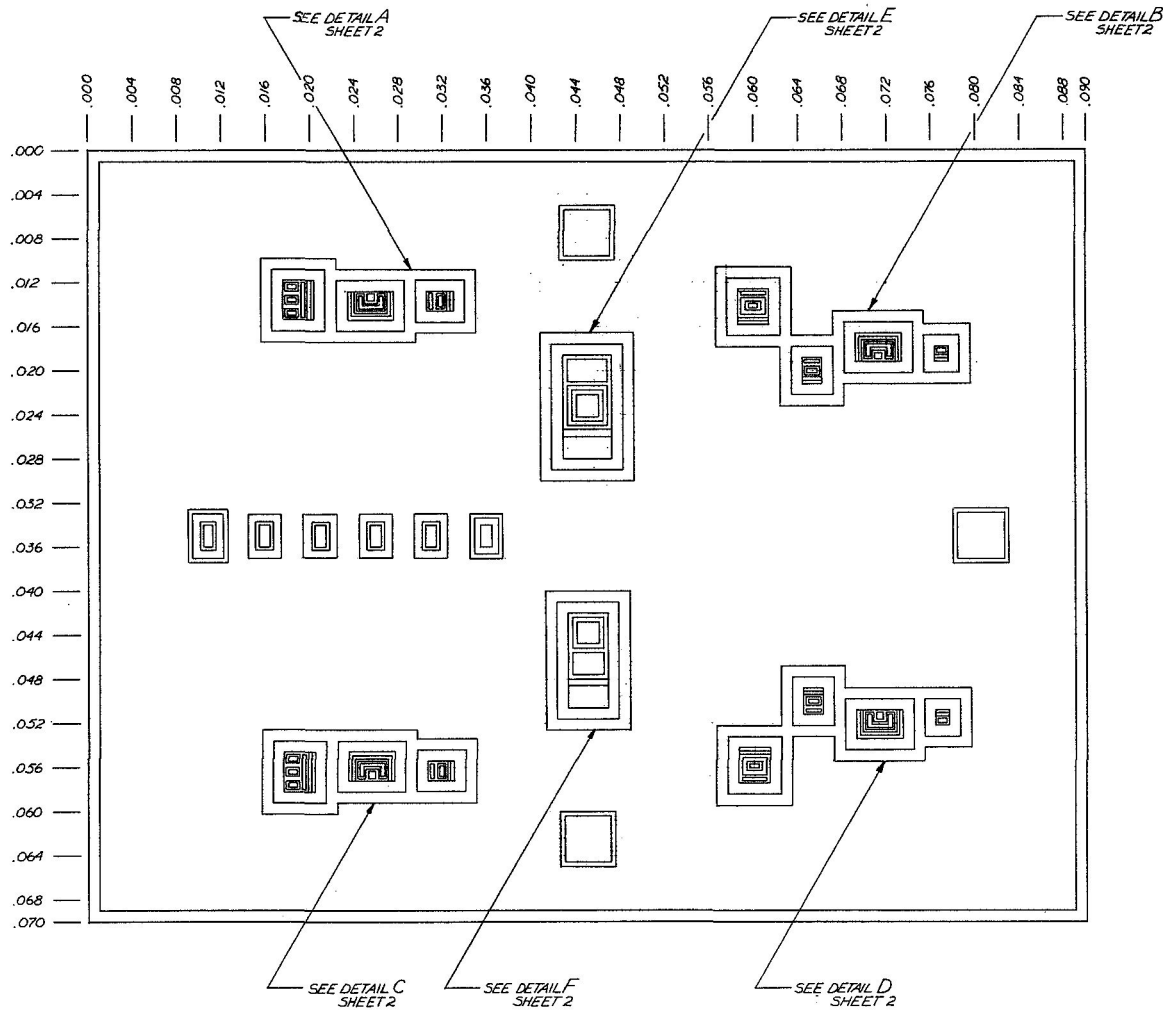


Figure 66. LSG Substrate

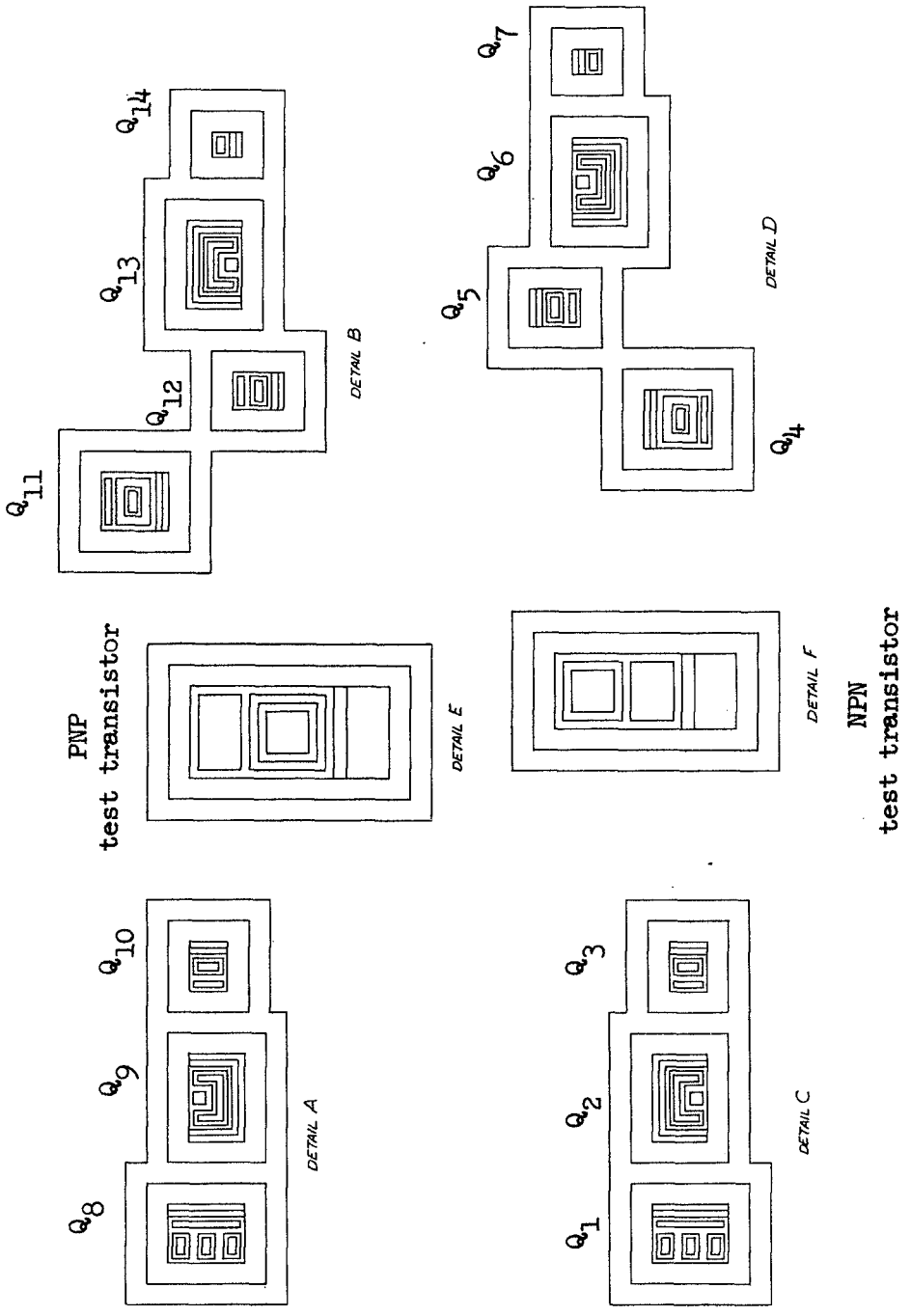


Figure 67. LSG Transistor Devices

Fig. 67. LSG Transistor Devices

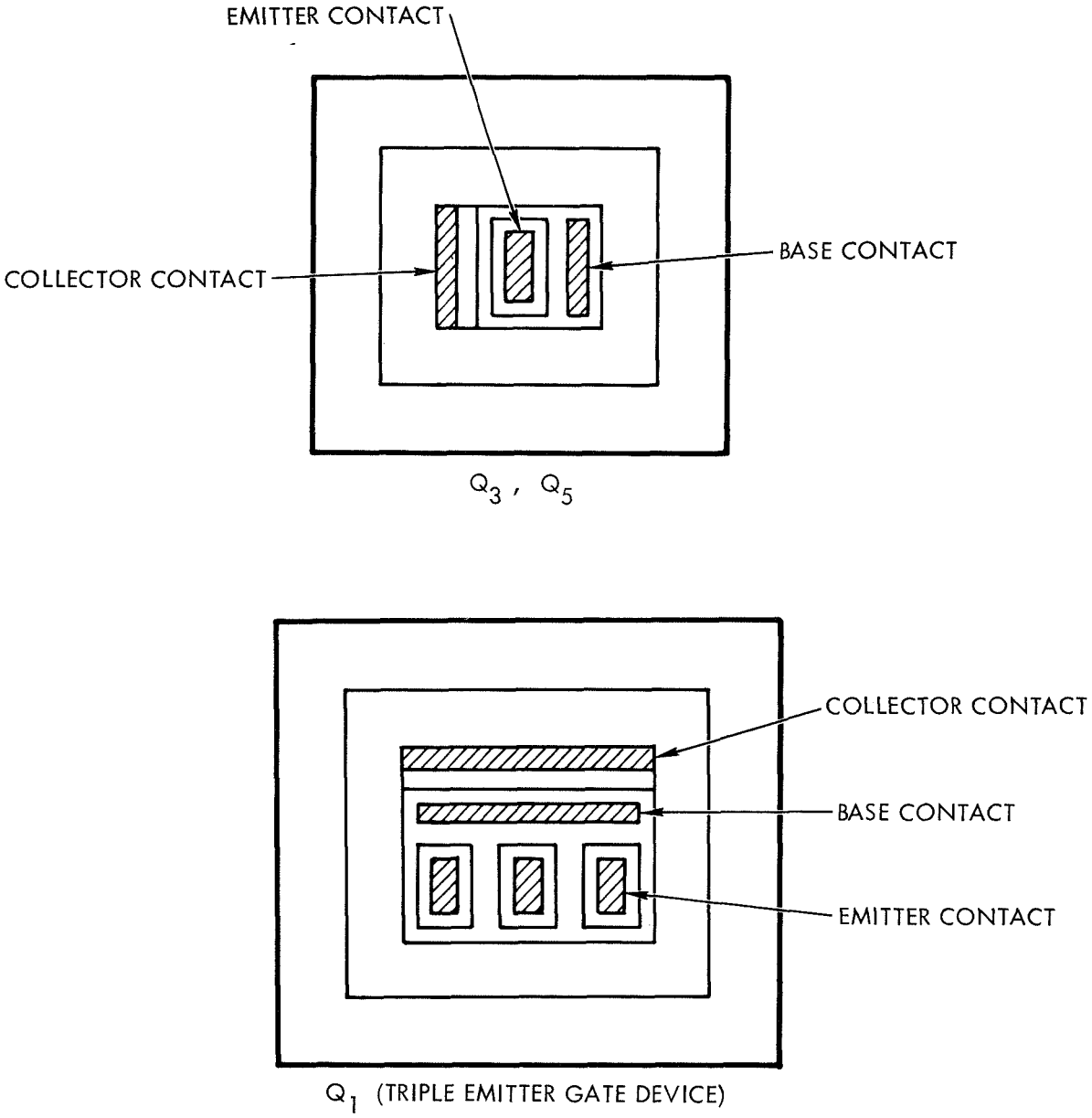


Figure 68. Transistor Device Geometry for Q1, Q3, and Q5

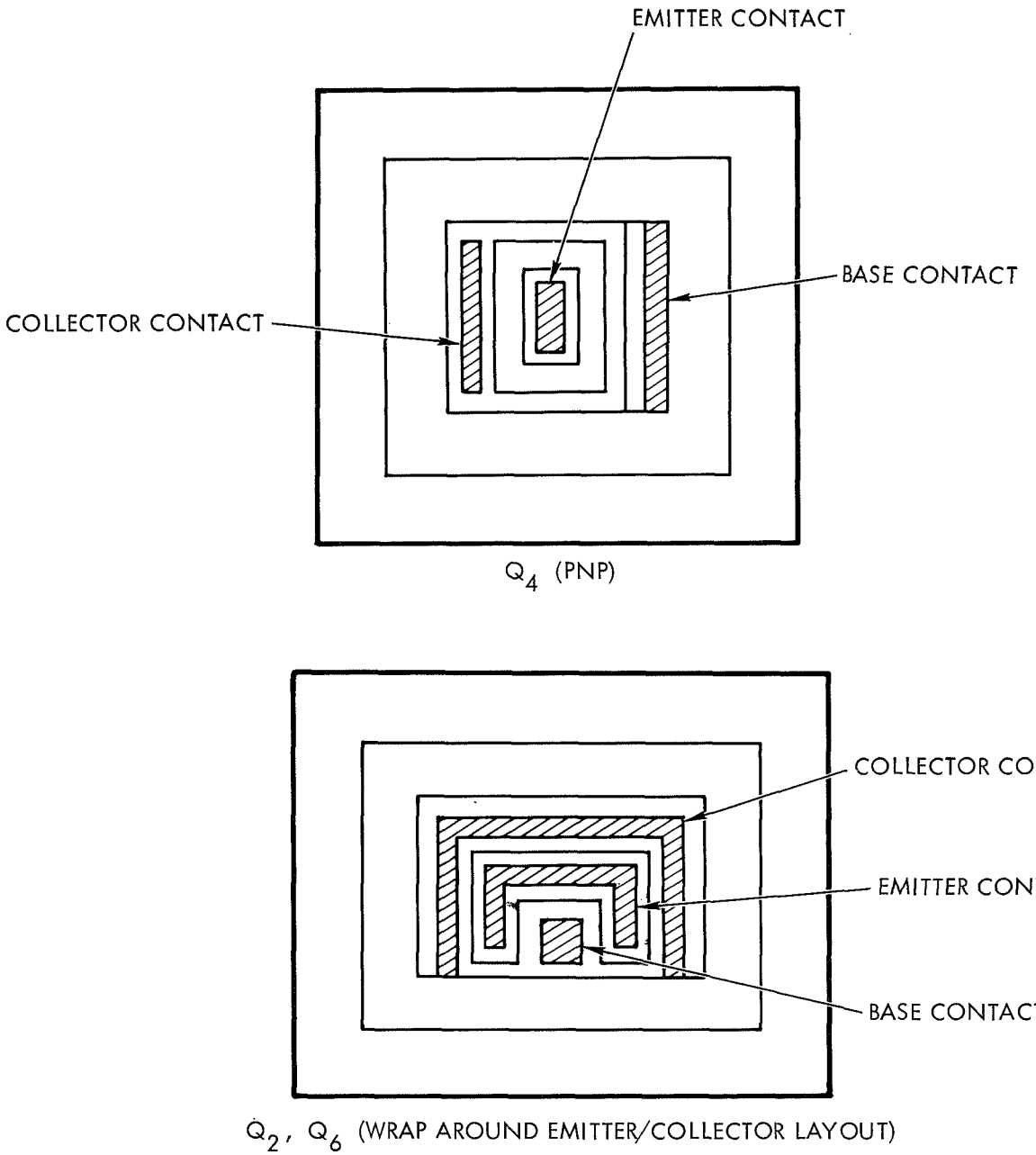


Figure 69. Transistor Device Geometry for Q2, Q4, and Q6

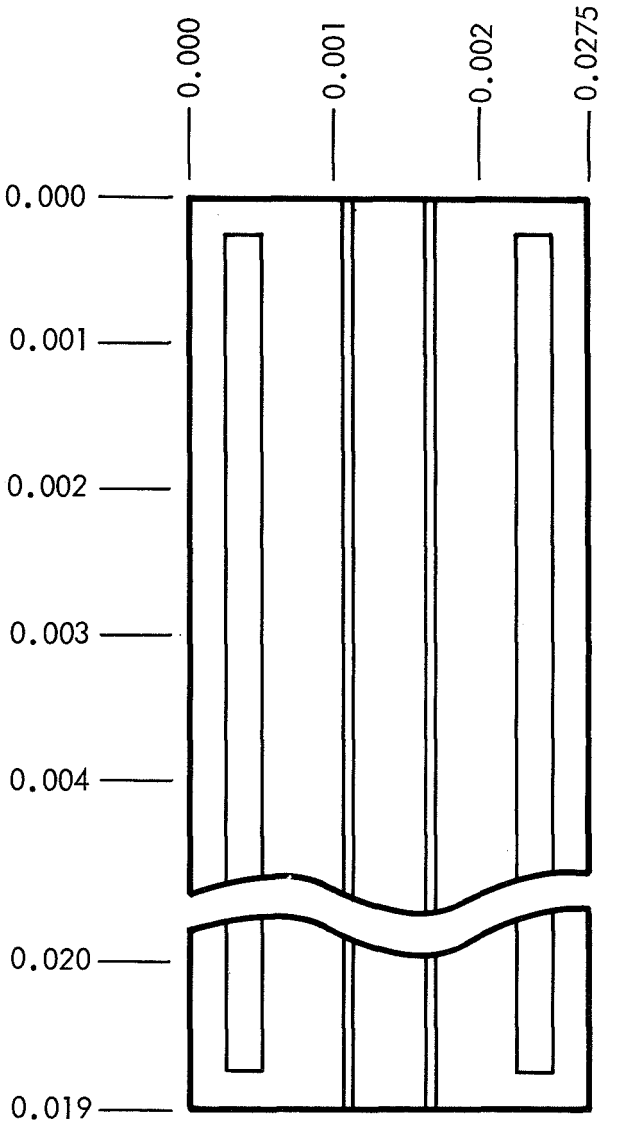


Figure 70. MM1 MOSFET Lateral Geometry

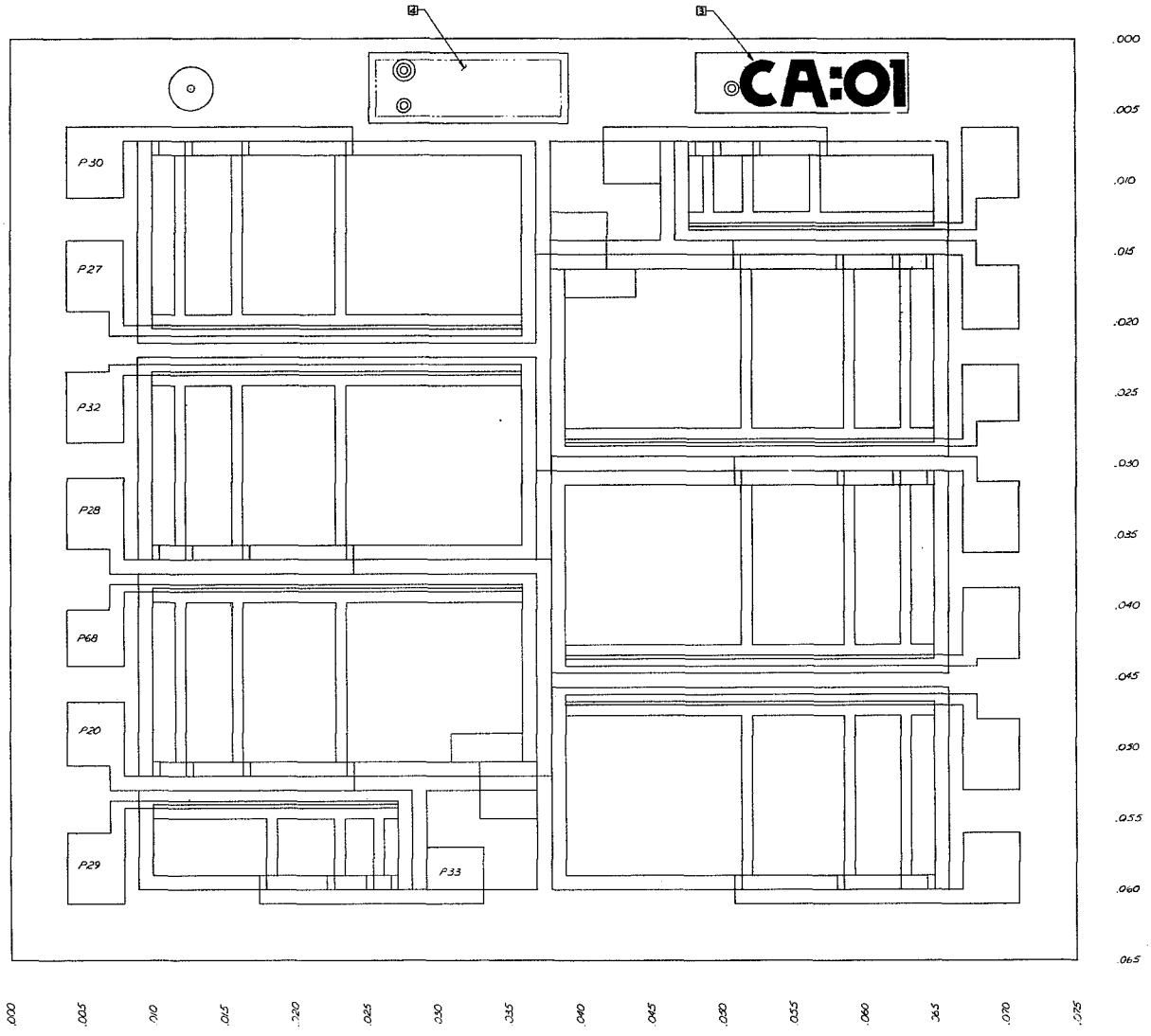


Figure 71. CA01 Lateral Geometry

through the metal. It melts and opens the shorting link. Figure 73 is a photograph of a fuse link before and after probing. Note how the aluminum melts and leaves a clean break in the interconnection pattern.

4.3 PACKAGING

Only the packaging of the TRW integrated circuit modules are considered in this section.

4.3.1 Packages

The following drawings specify the three types of packages used.

Figure 74: (1/4" x 1/4") flat pack - Used for the MM1

Figure 75: (1/4" x 3/8") flat pack - Used for the GTR, GMR, LSG

Figure 76: (3/8" x 3/8") flat pack - Used in the power converter

4.3.2 Die Attachment - Wire Bonding - Package Sealing

Two types of die attachment techniques were incorporated:

a) Thermal Bond. -Using a AuSi alloy as the bonding agent (GTR, GMR, MM1, LSG05)

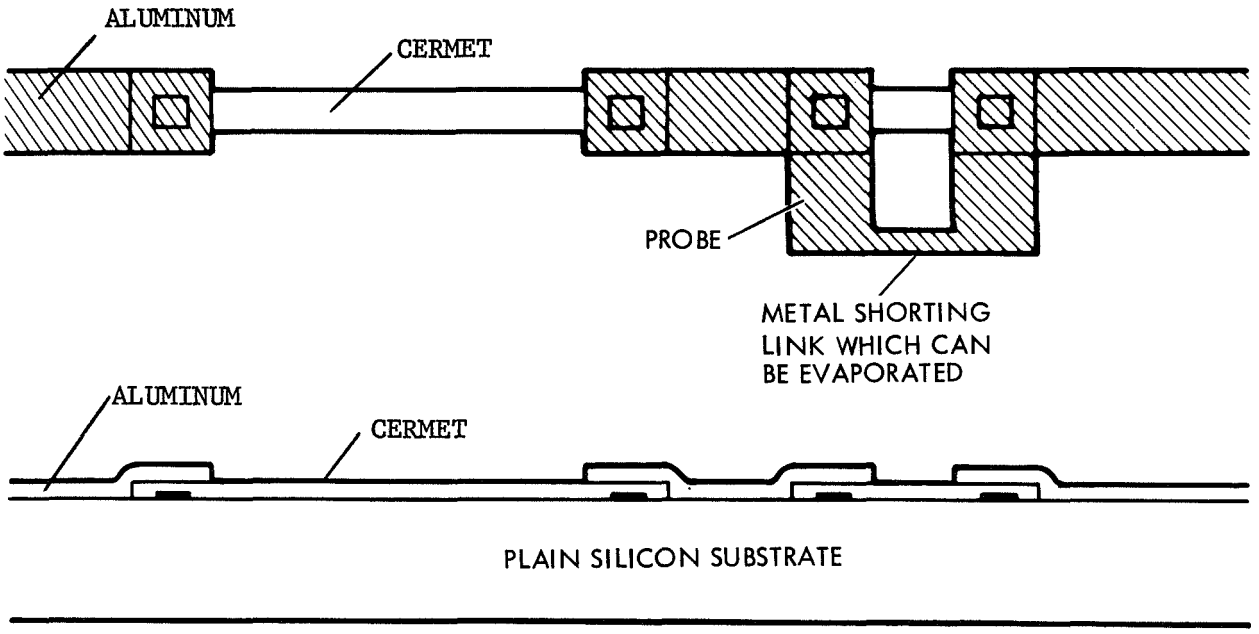
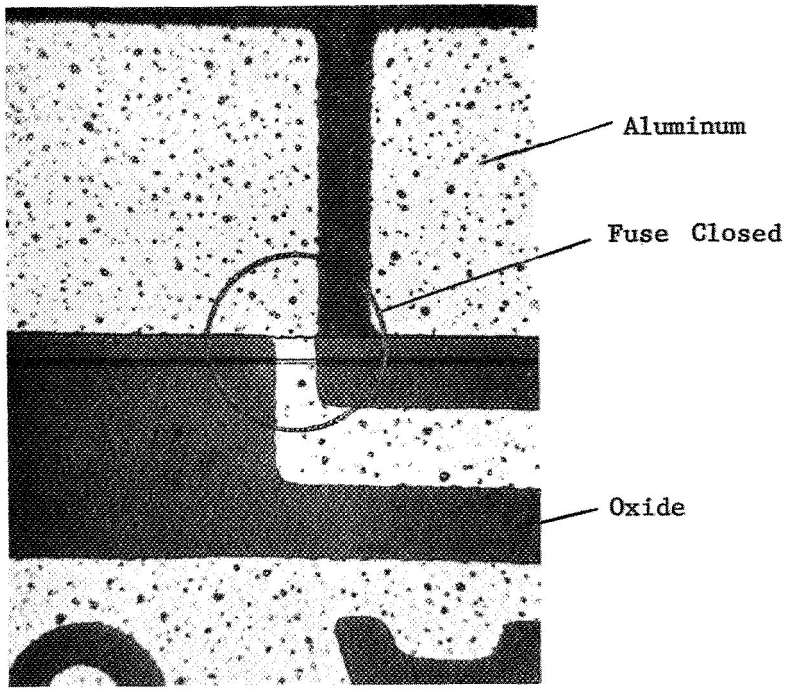
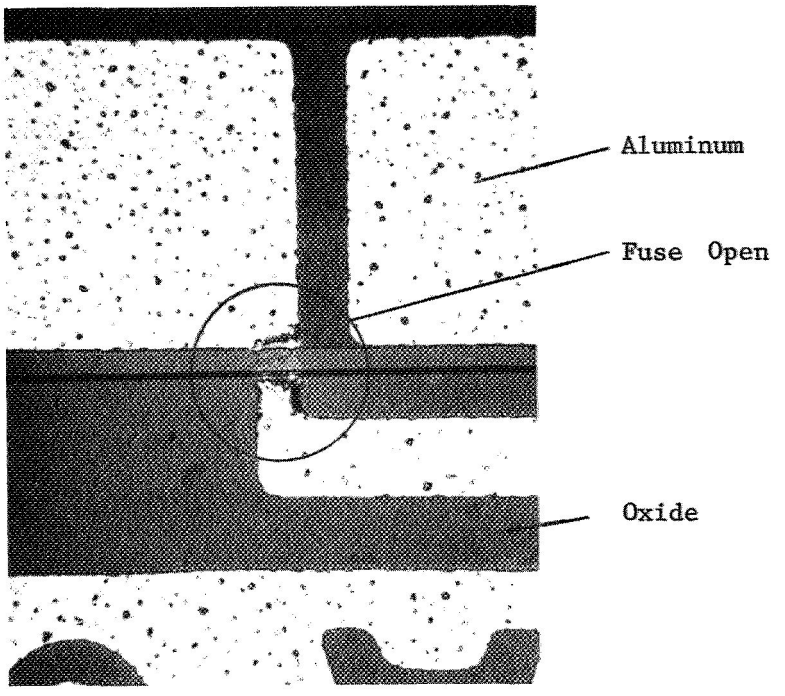


Figure 72. Typical Geometry of Adjustable Feedback Resistor



Before



After

Figure 73. Photograph of Fuse Link Operation

b) Conductive Epoxy Cermet. -Using DuPont Silver Preparation, Electronic Grade 5504-A, a high temperature epoxy (Power Converter flat pack)

The thermal bond is the preferred technique for establishing a reliable die attachment. The conductive epoxy is used only in applications in which the die must potentially be extracted and replaced in multi-die packages.

Thermal compression ballbonding with 1.5 mil gold wire is used for wire attachment. Sealing is accomplished using a gold alloy solder in an inert atmosphere.

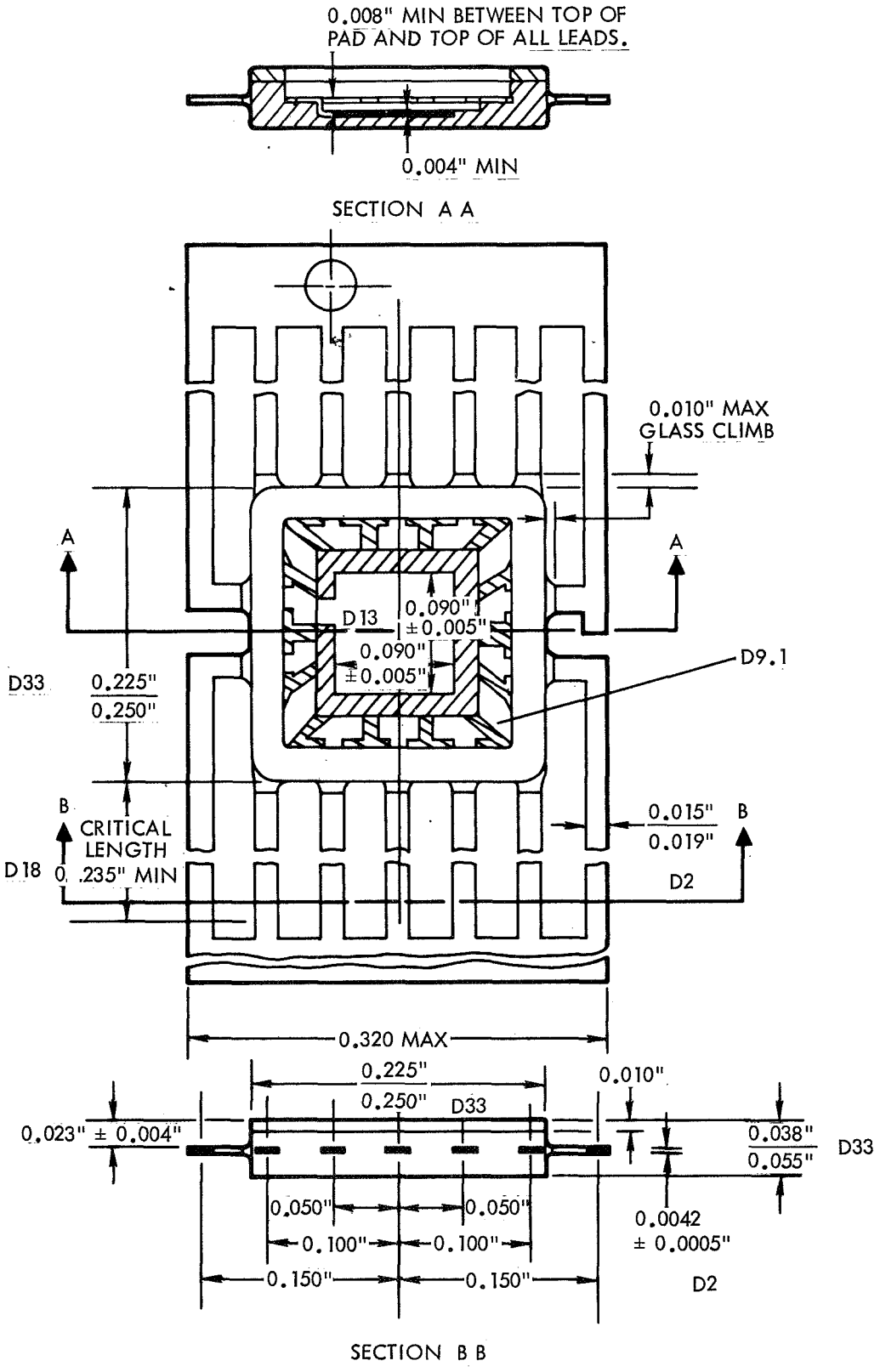
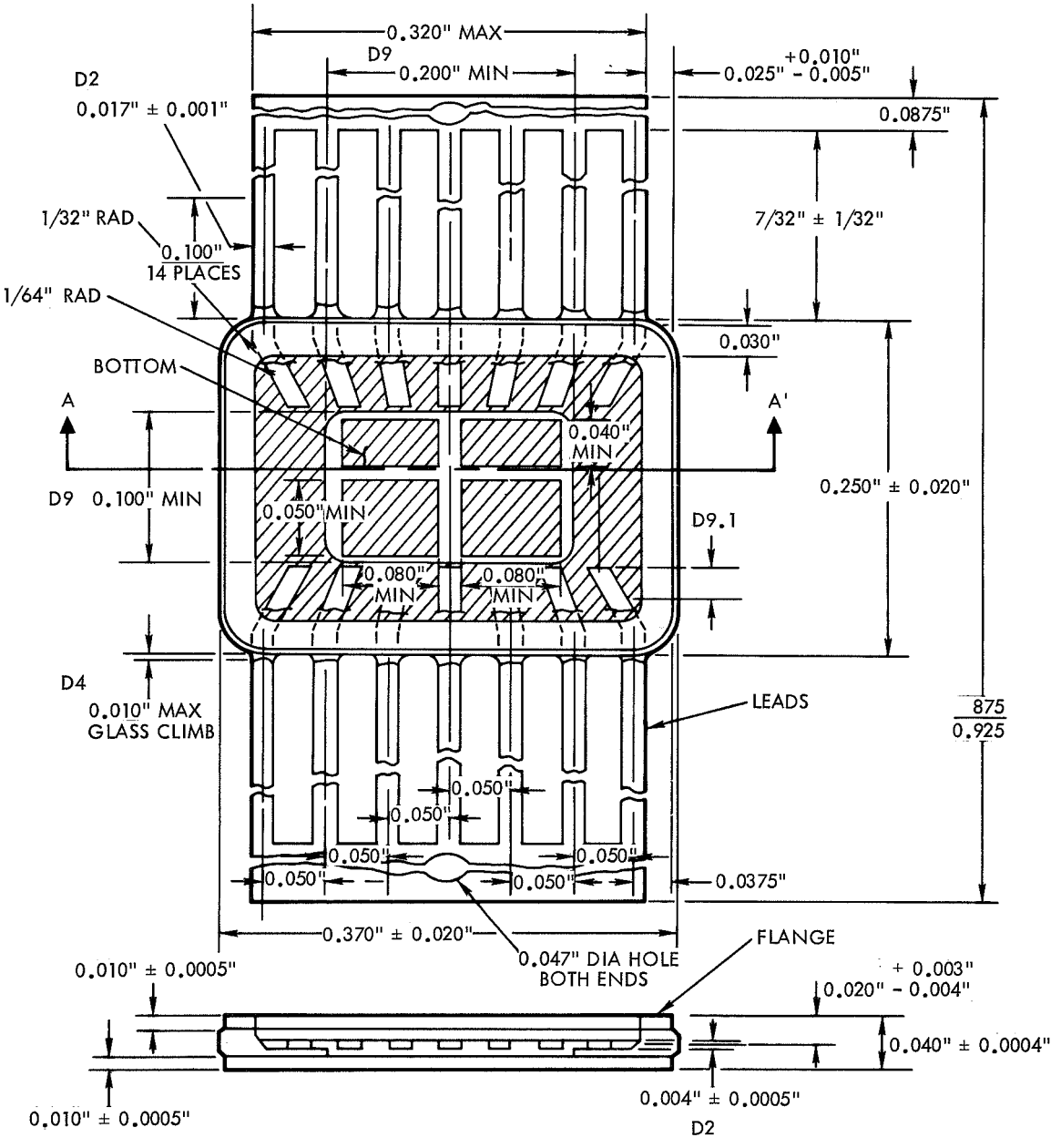


Figure 74. Flat Pack Drawing for MM1



SECTION A A

Figure 75. Flat Pack Drawing for GTR, GMR, and LSG

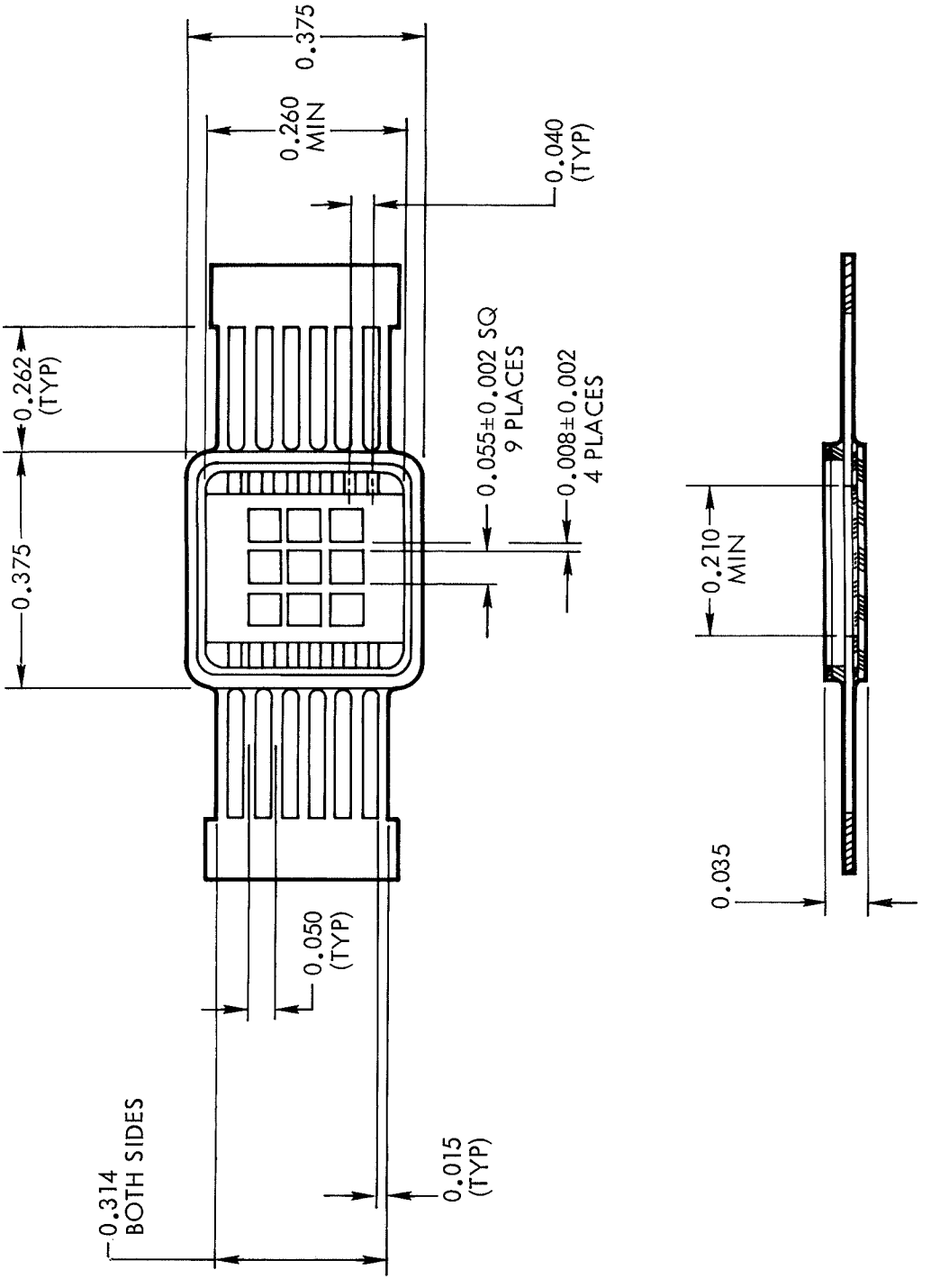


Figure 76. Flat Pack Drawing for Power Converter

5. TEST PROCEDURE

5.1 GENERAL

The purpose of this test procedure is to outline a sequence of functional tests to verify compliance with the contract specifications. The tests and results demonstrate the performance of the Power Programmer at TRW.

The following information includes the Contract Performance Specifications, which provide a correlation between measurements and contract objectives. The Test Specifications are a translation of the Contract Performance Specifications into a form suitable for final system breadboard functional tests. Note that the 90-channel Power Programmer is mechanized in a breadboard form with twelve functional channels plus two synchronization channels. The Test Specifications are written accordingly.

A description is given of the Power Programmer front panel to aid the operator in performing the tests, and finally the test procedure and Test Results demonstrate the operation of the final system breadboard.

Figure 77 shows the system block diagram. A power supply mounted on the system tester provides the +28 volts DC input. Test points are found on the tester front panel and/or the junction box (see Figure 80.) The gated regulator outputs and analog MOSFET inputs are brought out to the junction box to facilitate measurements taken at $-35^{\circ}C$ and $+95^{\circ}C$.

5.2 CONTRACT PERFORMANCE SPECIFICATIONS

NOTE: Numbering used on the following specifications is taken directly from the contract.

4. MISCELLANEOUS

4.1 Battery - The breadboard model shall be powered from an external battery. The characteristics of this battery are as follows:

4.1.1 The voltage is between 22 and 32 volts with 28 volts being nominal.

4.1.2 There is a possible maximum 4 volt peak-to-peak ripple (d-c to 2 kc square wave) impressed upon the battery voltage. The battery voltage, including the ripple, will be between 22 and 32 volts.

4.1.3 There is a possible transient on the power line that may reduce the battery voltage to as low as 0 volts or increase it to as high as 43 volts. This transient has a 20 millisecond base width duration and an 8 millisecond rise time.

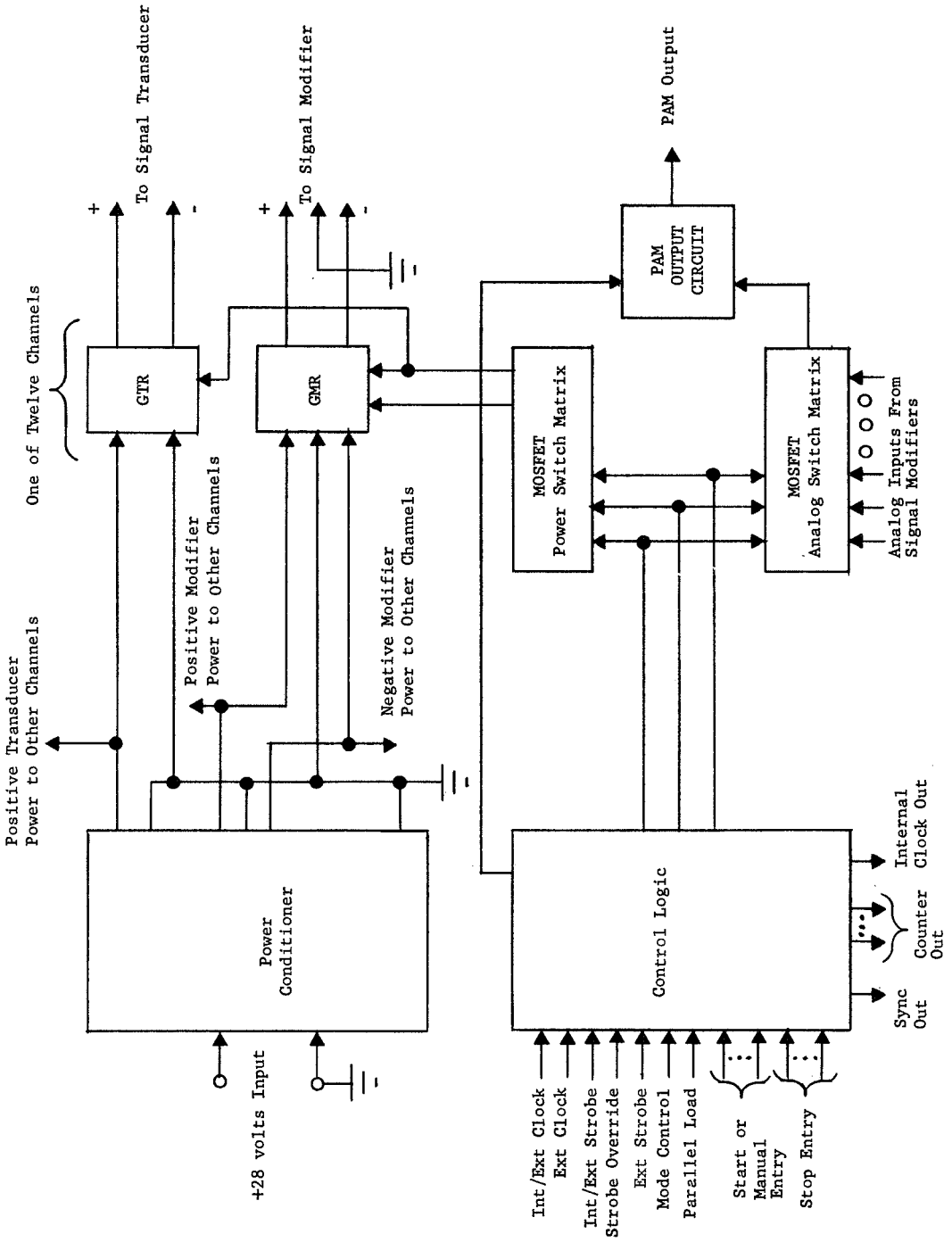


Figure 77. System Block Diagram

The circuitry connected to the battery is required to survive this transient, but the specification performance is not required. Operation shall return to normal within 100 microseconds after the duration of the pulse.

4.2 Service Life - The breadboard model shall be capable of operation within specifications for a minimum of 2000 hours, continuously or otherwise, during a service life of one year.

4.3 Warm up Time - The breadboard model shall be capable of operation within specifications after a warm up time not to exceed 0.5 minute.

4.4 Color - The breadboard model case shall be dull black.

4.5 Weight - The breadboard model shall be constructed with minimum weight. It shall demonstrate that a final programmer package, which includes all 90 channels, shall not weigh more than 1.2 pounds.

4.6 Volume - The breadboard model shall be constructed with minimum volume. It shall demonstrate that a final programmer package, which includes all 90 channels, shall not require a volume of more than 20.0 cubic inches.

4.7 External Connectors - External connectors shall be keyed to prevent mismating.

4.8 Reverse Polarity Protection - All items connected to the battery shall be protected from being destructed by polarity reversal and excessive battery current drain. Operation shall return to normal with proper polarity connections.

4.9 Product Marking - The breadboard model and all external connections shall be marked for identification purposes in a permanent manner.

4.10 Workmanship - Uniformity of shapes, dimensions, and performance shall provide interchangeability of the complete system.

5. PERFORMANCE SPECIFICATIONS

5.1 The breadboard model shall be designed to operate from the battery described by paragraph 4.1. Power shall be sequentially supplied to external signal modifiers, and the single ended outputs of these modifiers, which have a voltage of 0 to +5 volts at a frequency of dc to 1 kc, shall be gated to a single point.

5.1.1 Number of Channels - The programmer logic shall accommodate up to 90 channels, 88 signal channels and 2 frame identification channels. The breadboard will include only 12 complete channels. The design shall be such that any lesser combinations of channels may be obtained by strapping together any combination of channels.

5.1.2 Sample Rate - The nominal sample rate shall be 900 channels per second. The programmer shall be capable of generating up to 12,500 channels per second.

5.1.3 Synchronization - The synchronization to an external oscillator shall be accomplished with the application of a synchronizing pulse.

5.1.4 Wave Train Identification - Two channels shall be used for identification and synchronization purposes according to IRIG specifications on PAM frame identification (50% duty cycle signals).

5.1.5 Cross Talk and Ripple - The maximum output ripple due to cross talk and other internal conditions shall be 25 millivolts peak-to-peak as measured with an oscilloscope having a pass band of 15 megacycles.

5.1.6 Stability - The error of the signal modifier output signal due to the gating to a single point shall not exceed $\pm$ 1%.

5.1.7 Rise Time - The rise time of the programmer shall be such that the power to the signal modifiers and the gated output signals will reach its value in less than 50 microseconds.

5.1.8 Signal Modifier Power - The breadboard shall supply commutated power to each channel, which includes an amplifier and a transducer as described on Contract NAS 9-4640. The voltage shall be transformer isolated from the battery which is described by paragraph 4.1.

5.1.9 Power Requirements - The breadboard model shall not require more than 200 ma when operated from a 28 volt battery.

5.1.10 Power Line Feedback - The feedback ripple from the breadboard model to the battery shall be no more than 30 millivolts peak-to-peak as measured across a one ohm resistor in series with the battery when measured by an oscilloscope having a pass band of 15 megacycles.

5.1.11 Logic Commands - The logic commands shall include the following types:

a. Clock Control (Internal or external sync., stop on any channel, all or any sequential portions of channels per frame.)

b. Strobe Control (Selection of duty cycle per channel time, 50 $\pm$ 5 per cent for normal PAM use.)

c. Mode Control (Normal serial output or forced random selection of channels.)

5.1.12 Amplifier Power - The amplifier power shall be on for one sample period in advance of the output sample period.

5.3 TESTER FRONT PANEL (DESCRIPTION)

The following section describes the function of the front panel controls of the PPT (Power Programmer Tester). Refer to Figure 78. The operator can insert various digital control signals and monitor the resultant channel position and/or PAM output via the front test panel. Note that digital input is activated by an equivalent switch closure to ground. System commands are therefore simulated by switch positions.

5.3.1 Indicator Lights

The programmer channel position, 0 through 127, is displayed as a binary number on the row of seven lights appearing at the top of the front panel. An ON light represents a 1 and an OFF light represents a 0.

5.3.2 Auto Start Channel - Manual Entry

The seven switches labeled "Auto Start Channel" provide the binary input for selecting a channel in the random access mode of operation and also for selecting the start channel in the sequential mode of operation.

5.3.3 Auto Stop Channel (N-1)

The seven switches labeled "Auto Stop Channel (N-1)" provide the binary input for selecting the stop channel in the sequential mode of operation. The actual stop channel is the number represented by the switch positions plus one. The override switch causes the programmer to cycle from the start channel all the way through to the last channel (channel 127), when the switch is in the up position, regardless of the position of the other seven switches.

5.3.4 Mode

The mode switch (toggle) selects the Power Programmer mode of operation as follows:

(MAN) ≡ manual or random access mode of operation.

(AUTO) ≡ automatic or sequential mode of operation.

The push button manual switch (MAN/LOAD) is used to load the counter with the channel position selected on the (MANUAL ENTRY) input switches.

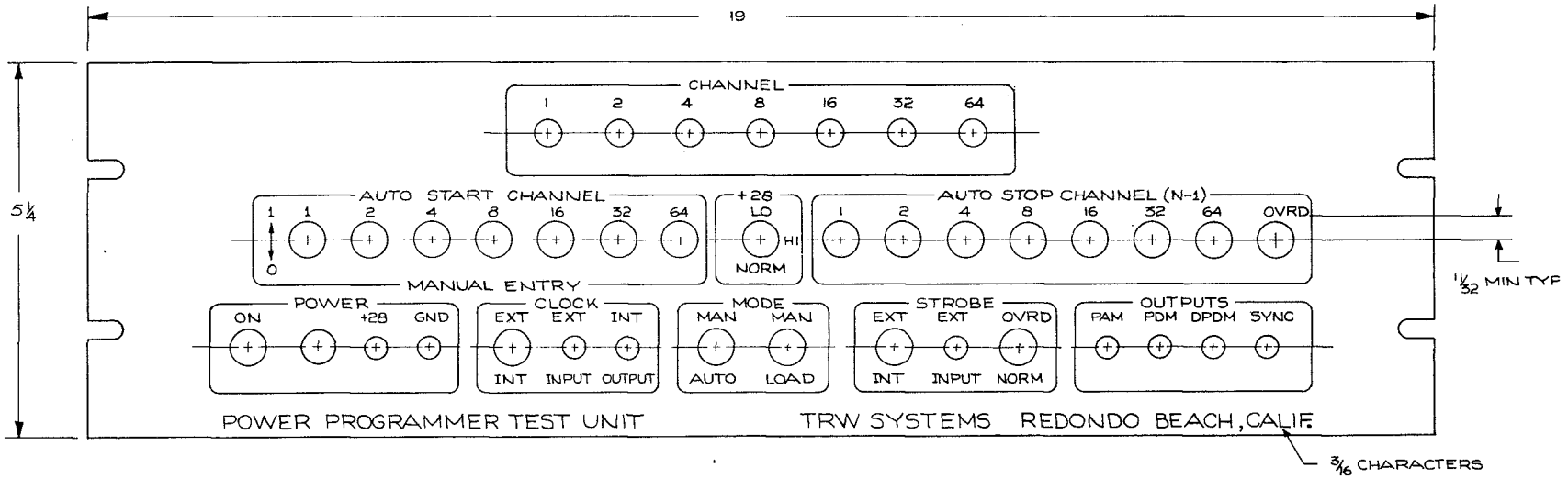


Figure 78. Power Programmer Tester Front Panel

5.3.5 Strobe

The strobe signal determines the analog output sample period. The (EXT/INT) toggle switch selects the 50% duty cycle internal strobe signal, or an external strobe signal via the (EXT/INPUT) connector. In the external strobe mode, analog sampling will occur when the signal is at the logic 1 level. (Minimum pulse duration at logic 1 level is 400 nsec. The frequency range is DC to 100 KHz.) The strobe override switch (OVR/NORM) provides a continuous active level for the strobe signal as follows:

(OVR) ≡ override condition, equivalent to a logic 0 input.

(NORM) ≡ no effect on programmer, equivalent to a logic 1 input.

5.3.6 Power

A power supply is included in the tester to convert 110 volts/ 60 Hz AC to +28 volts DC. A switch, labeled (+28), in the center of the front panel allows the operator to select the specified tolerances on the +28 volts as follows:

HI	+ 32 volts
LO	+ 22 volts
NORM	+ 28 volts

The power switch, which interrupts the 110 volt/60 Hz AC input, and power light indicator are located in the bottom left-hand corner of the front panel. The terminals (+28) and (GND) monitor the DC power input to the Power Programmer. (Note, do NOT connect an external power supply to these terminals.)

5.3.7 Clock

The switch located in the clock section selects an internal 900 Hz clock (INT) or an external clock signal (EXT). When the switch is in the (EXT) position and a signal generator connected to the (EXT INPUT) terminal, the programmer steps to the next channel on transition from logic 1 to logic 0 at a rate which is one-tenth of the signal generator rate. The (INT OUTPUT) terminal monitors the 900 Hz, 50% duty cycle square wave internal clock. It can be used for synchronization or test purposes. Note: if the PAM format is used, analog data is sampled during the positive half of INT CLK OUT wave form.

The external clock input specifications are:

Sine wave:	Amplitude:	2 V rms minimum
		3 V rms nominal
		10 V rms maximum

	Frequency:	DC to 150 KHz
Rectangular Wave:	Amplitude:	-3 volts negative minimum +5 volts positive nominal +15 volts positive maximum
	Positive Pulse Duration:	1 microsecond minimum
	Frequency:	DC to 150 KHz

5.3.8 Outputs

The PAM output is monitored on the front panel terminal. (Minimum load resistance is 50 K ohms. Maximum load capacitance is 1000 pF.) The output terminals marked PDM and DPDM are not presently used, but are available for future use in the event that the PDM and DPDM circuits are added to the output circuit board. The (SYNC) terminal provides one pulse every frame period. This logic 1 level pulse occurs during the second half of the (N-1) channel period and during all of the (N) channel period where N denotes the last program channel. (See Figure 79.)

5.4 TEST SPECIFICATIONS

Figure 79(a) shows the Power Programmer output which conforms to the IRIG specified PAM pulse train wave form. An increasing staircase is shown and is obtained by inserting the AI-3 card into card file position 13. Figure 79(b) shows the gated regulator output waveforms. (Note: For discussion of system operation, the initial 50% of the channel period will be the OFF period. IRIG specifies the initial 50% of the channel period as ON period; however, the difference is only academic. The waveforms are identical.) The following specifications apply to the Power Programmer final test.

5.4.1 Logic Commands and Function

The logic commands shall include the following types:

5.4.1.1 Mode Control - The mode of operation shall be either serial or parallel.

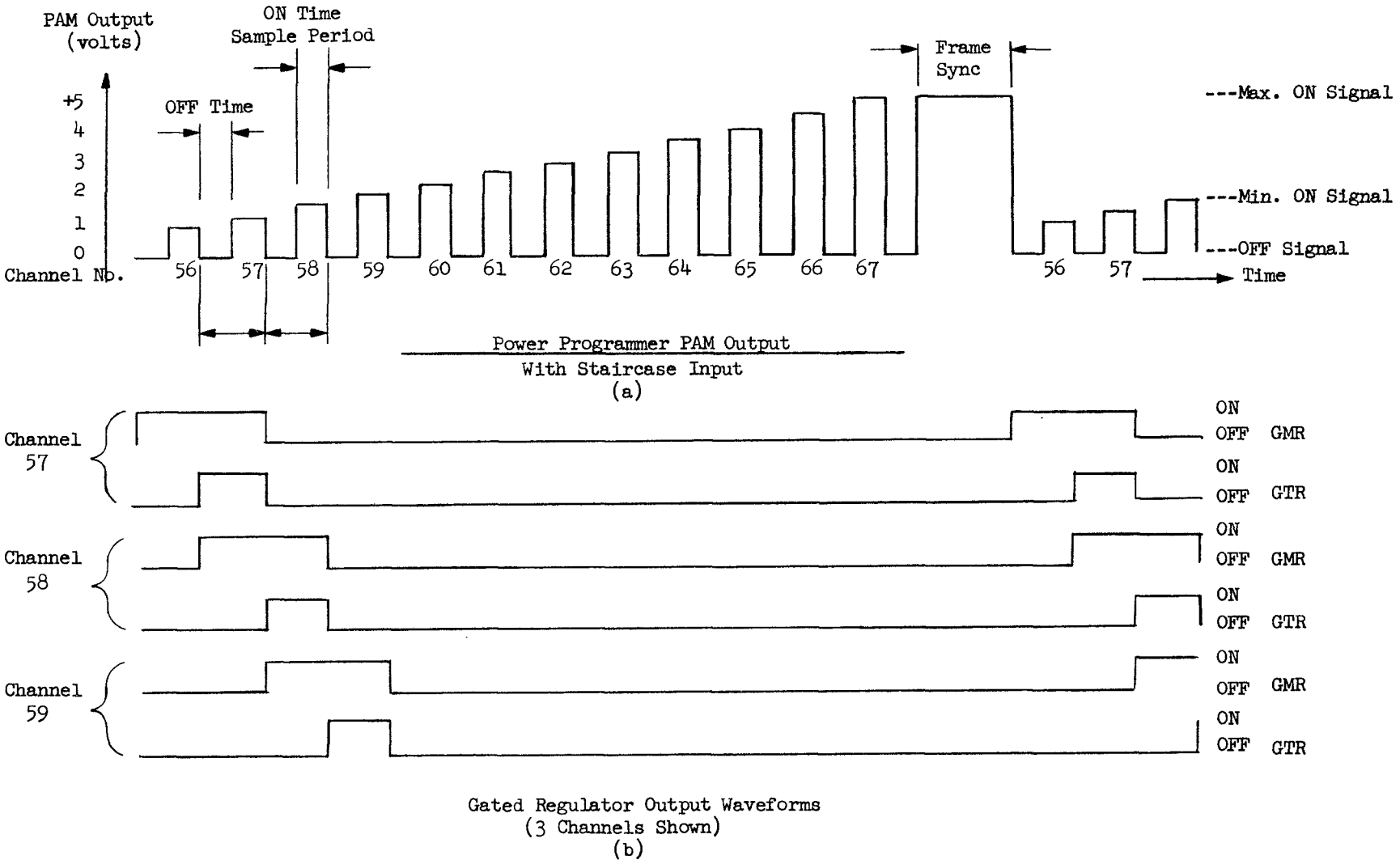


Figure 79. Power Programmer Output

5.4.1.2 Serial Operation - The programmer shall sequence through a minimum of 3 and a maximum of 14 channels, the last two channels being reserved for synchronization. The start and stop channels shall be externally selectable. A PAM synchronization pulse will identify each frame according to IRIG specifications.

5.4.1.3 Parallel Operation - The programmer shall operate in a parallel (or random access) mode, such that any channel $56 \leq N \leq 67$ can be selected and held.

5.4.1.4 Clock Control - An internal or external clock shall be selectable. The internal clock shall be 900 cps $\pm$ 3%.

5.4.1.5 Strobe Control - An internal or external strobe signal shall be selectable. (The strobe signal determines the analog output sample period.) The internal strobe signal shall provide a 50 $\pm$ 3% duty cycle for normal PAM use.

5.4.1.6 The programmer logic shall operate up to 12.5 KHz.

5.4.2 Synchronization

The PAM synchronization pulse shall be internally generated with an amplitude of 5 volts $\pm$ 1% and shall occur during the ON time of the (N-1) channel and during the ON and OFF time of the (N) channel, where N denotes the last programmed channel.

5.4.3 Duty Cycle

The PAM duty cycle shall be 50 $\pm$ 3% where

$$\text{Duty Cycle} \equiv \frac{\text{ON Sample Period}}{\text{Channel Period}} \times 100\%$$

5.4.4 Channel Period

The PAM channel period shall be 1110 $\pm$ 50μsec. For a full 90-channel system, the frame rate is 10 frames per second.

5.4.5 Zero Data Pedestal

With a channel input of zero volts, the PAM pulse amplitude shall be 1 ± 0.050 volts.

5.4.6 Full Scale Output Amplitude

For a full scale amplifier output voltage of +5.000 volts, the PAM pulse amplitude shall be +5 ± 0.050 volts.

5.4.7 Pulse Amplitude Stability

The amplitude of any PAM channel output pulse shall remain constant within ± 1% of full scale under all electrical and environmental conditions specified.

5.4.8 OFF Time Voltage

The level of the PAM output between sample periods shall be zero ± 0.050 volts.

5.4.9 Ripple and Cross Talk

The maximum output ripple due to cross talk and other internal conditions shall be 25 millivolts peak-to-peak as measured with an oscilloscope having a pass band of 15 megacycles.

54.10 Transducer Power

Each of the 12 channels shall have gated power to excite a transducer. The following specifications apply.

5.4.10.1 The transducer power shall be gated ON during the entire channel period corresponding to the selected output channel period.

5.4.10.2 The transducer power shall reach 99% of its final value in less than 50 μsec.

5.4.10.3 The transducer power shall excite a 350 ohm ± 5% transducer with 10 volts ± 50 millivolts, when subjected to specified battery fluctuations and environment.

5.4.10.4 The ripple on the transducer power shall not exceed 25 millivolts peak-to-peak as measured with an oscilloscope having a pass band of 15 megacycles.

5.4.11 Signal Modifier Power

Each of the 12 channels shall have gated power to excite a signal modifier. The following specifications apply.

5.4.11.1 The signal modifier power shall be gated ON during two entire channel periods, the channel period corresponding to the selected channel plus the previous channel period.

5.4.11.2 The signal modifier power shall reach 99% of its final falue in less than 50 μsec.

5.4.11.3 The signal modifier power shall excite a signal modifier with 30 $\pm$ 0.30 volts drawing 6 ma of current, when subjected to specified battery fluctuations and environment.

5.4.11.4 The ripple on the signal modifier power shall not exceed 25 millivolts peak-to-peak as measured with an oscilloscope having a pass band of 15 megacycles.

5.4.12 Power Requirements

The Power Programmer shall receive power from a +28 volt source. The related specifications include:

5.4.12.1 The Power Programmer shall meet the stated specifications with input voltage variations from 22 to 32 volts.

5.4.12.2 The Power Programmer shall be protected from being destroyed by polarity reversal and excessive battery current drain. Operation shall return to normal with proper polarity connections.

5.4.12.3 There is a possible maximum 4 volt peak-to-peak ripple (DC to 2 kc square wave) impressed upon the battery voltage. The battery voltage, including ripple, will be between 22 and 32 volts.

5.4.12.4 There is a possible transient on the power line that may reduce the battery voltage to as low as 0 volts or increase it to as high as 43 volts. This transient has a 20 millisecond base width duration and an 8 millisecond rise time. The circuitry connected to the battery is required to survive this transient, but the specification performance is not required. Operation shall return to normal within 100 microseconds after the duration of the pulse.

5.4.12.5 The feedback ripple from the breadboard model to the battery shall be no more than 30 millivolts peak-to-peak as measured across a one ohm resistor in series with the battery when measured by an oscilloscope having a pass band of 15 megacycles.

5.4.12.6 The breadboard model shall not require more than 200 milliamps when operated from a 28 volt battery.

5.4.13 Temperature

The Power Programmer shall operate to specifications over the temperature range of $-35^{o}C$ to $+95^{o}C$.

5.5 TEST PROCEDURE

The test configuration shown in Figure 4 shall be used for the Power Programmer test procedure. The test equipment list is given in Table I. The entire procedure is first conducted at $+25^{o}C$ and then repeated at $+95^{o}C$ and $-35^{o}C$. Note: A dehumidified temperature chamber must be used to prevent possible system failure due to condensation of water vapor.

5.5.1 Digital

This portion of the test procedure checks the digital control section of the Power Programmer, thereby verifying compliance with Test Specification 1, Logic Commands.

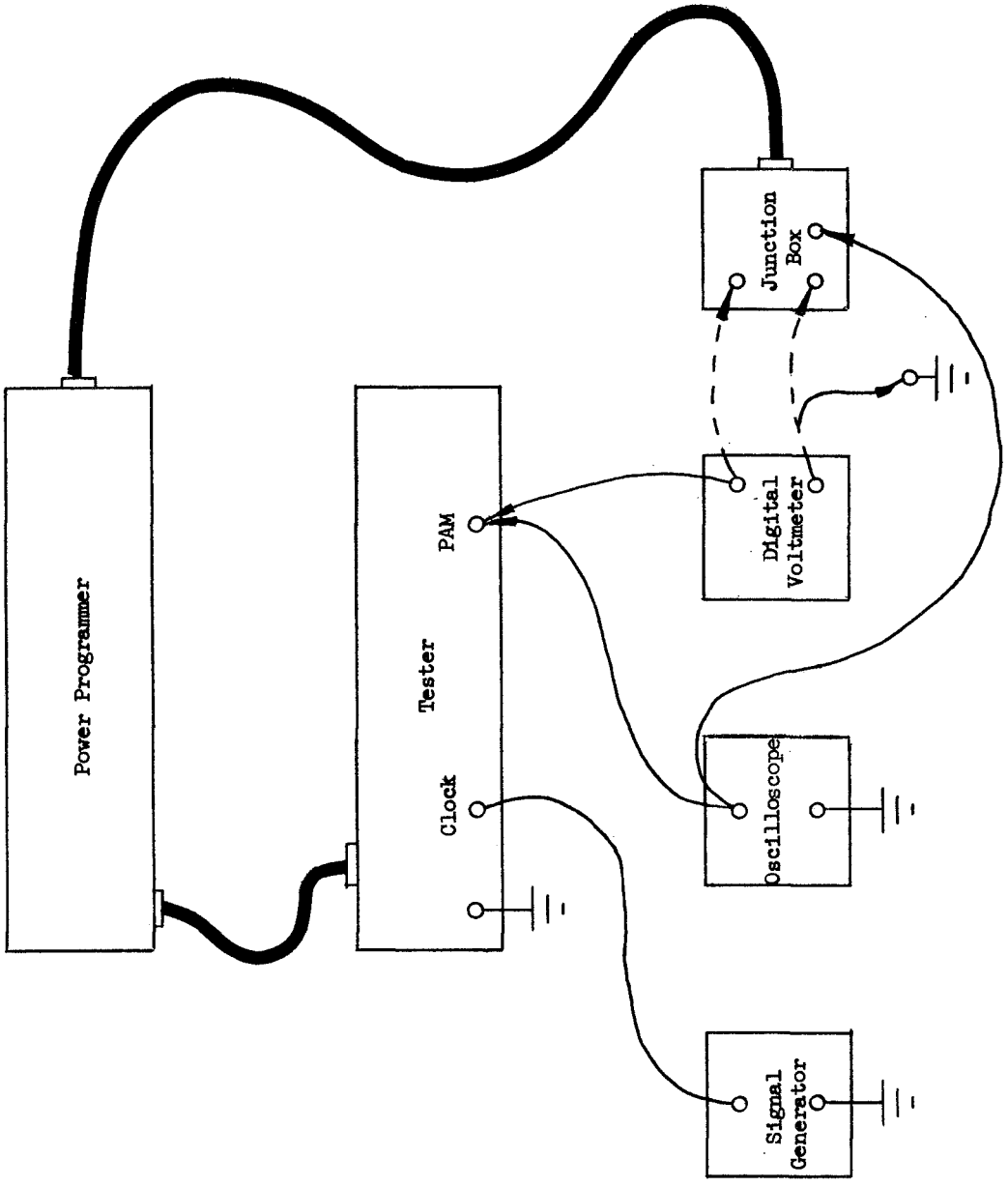


Figure 80. Test Configuration

TABLE 5-I. TEST EQUIPMENT

1	Cathode Ray Oscilloscope	Tektronix Model 545A or equivalent
1	Dual-Trace Oscilloscope Preamp	Tektronix Model CA or equivalent
1	Digital Voltmeter	Hewlett-Packard Model 2401 Dymec Integrating Digital Voltmeter or equivalent
1	Signal Generator	Hewlett-Packard Model 650A or equivalent

5.5.1.1 Channel 0 to 127 Sequencing

(1) Connect the signal generator to the external clock input and adjust the signal generator for 10 Hz and approximately 3 V RMS. (Note that the Ext clock frequency is divided by 10.)

(2) Set the PPT (Power Programmer Tester) as follows:

(a) Ext/Int Clock - Set Ext
(b) MAN/AUTO Mode - Set AUTO
(c) Ext/Int Strobe - Set Int
(d) Ovrd/Norm Strobe - Set Norm
(e) Auto Start Channel, 0000000 (Channel 0)
(f) Auto Stop Channel (N-1), 0000000 (Channel 1)
(g) Auto Stop Channel Override Active (UP)
(h) +28 - Set Norm
(i) Power - Set ON

(3) Power Programmer will then automatically sequence from channels 0 to 127 at 1 Hz. Visually monitor the indicator lights to verify proper sequencing from channel 0 to channel 127.

	-35°C	+25°C	+95°C
Proper Sequencing	✓	✓	✓

5.5.1.2 Stop and Start Check In The Sequential Mode

(1) Set the PPT as follows:

(a) Auto Start Channel, 0000000 (Channel 0)
(b) Auto Stop Channel (N-1), 0000000 (Channel 0)
(c) Auto Stop Override Inactive (Down)
(d) All other controls as indicated in 5.5.1.1(2).

(2) Monitor lights to verify sequencing between channels 0 and 1.

(3) Repeat (1) and verify sequencing for the following channels. (Note: STOP channel is channel N, not channel (N-1).)

Start Switches	Lights Start on Channel	Stop (N-1) Switches	Lights Stop on Channel
1000000	1	1000000	2
1100000	3	1100000	4
1110000	7	1110000	8
1111000	15	1111000	16
1111100	31	1111100	32
1111110	63	1111110	64
1111111	127	1111111	0

	-35°C	+25°C	+95°C
Proper Sequencing	✓	✓	✓

5.5.1.3 Check of Random Access Mode

(1) Set the PPT as follows:

(a) Manual Mode (UP)
(b) Manual Entry, 0000000
(c) Auto Stop Override, Active - Set Ovrd

(2) Press Manual Load

(3) Monitor lights to verify correlation with Manual Entry. (Note: "1" indicates light on, "0" indicates light off.)

(4) Repeat(1), (2), and (3) for the following Manual Entry:

Manual Entry
1000000
0100000
0010000
0001000
0000100
0000010
0000001

(5) If the lights correlate properly in each case, the set-reset function has been checked for the counter in the random access mode, verifying proper operation in random access mode.

	-35°C	+25°C	+95°C
Proper Operation	✓	✓	✓

5.5.1.4 Check the Sync Output Signal

(1) Set the PPT as follows:

(a) Ext/Int Clock - Set Int
(b) Man/Auto Mode - Set Auto
(c) Ext/Int Strobe - Set Int
(d) Ovrd/Norm Strobe - Set Norm
(e) Auto Start Channel, 0001110 (Channel 56)
(f) Auto Stop Channel (N-1), 0010001 (Channel 68)
(g) Auto Stop Channel Override: Inactive

(2) Connect the oscilloscope preamplifier input to the sync output terminal and sync on the positive going edge.

(3) Monitor the waveform on the scope. The pulse should be approximately 1670 microseconds wide and spaced every 15.5 milliseconds.

	-35°C	+25°C	+95°C
Sync Signal	✓	✓	✓

5.5.1.5 Check Operation of the Programmer Logic at 12.5 kHz

(1) Connect the oscilloscope to the MOS OUT terminal on the junction box. Connect SYNC output on PPT to delayed trigger input on scope and sync on negative going edge of SYNC signal.

(2) Set the PPT as follows:

(a) Ext/Int Clock - Set Ext
(b) Man/Auto Mode - Set Auto
(c) Ext/Int Strobe - Set Ext
(d) Ovrd/Norm Strobe - Set Norm
(e) Auto Start Channel, 0001110 (Channel 56)
(f) Auto Stop Channel (N-1), 0010001 (Channel 68)
(g) Auto Stop Channel Override Inactive (Down)

(3) Adjust the signal generator for 150 kHz and 3 V RMS.

(4) Insert the stairstep function card (AI-3) into the junction box. (Note: The AI-J card MUST be inserted in card file position 13 to allow use of other AI cards in the junction box.) CAUTION: Remove power before inserting or removing any card.

(5) Reapply power and monitor the waveform on the oscillos oscilloscope to verify that the analog signal assumes 99% of its final value in less than 40 μsec.

	-35°C	+25°C	+95°C
Operates properly at 12.5 kHz	✓	✓	✓

5.5.2 PAM Output

This portion of the test procedure checks the IRIG specified PAM output, thereby verifying compliance with Test Specifications 2 through 9. Note that the analog voltage accuracies will be made on a DC basis to simplify measurements. If the DC analog level is assumed identical with the asymptotic analog level in the sequential mode, a valid accuracy versus time measurement can be made with an oscilloscope to verify the accuracy in the sequential mode.

5.5.2.1 Check PAM Output General Waveform

(1) Connect the oscilloscope to the PAM output terminal on the PPT. Synchronize the oscilloscope on the negative going edge of the SYNC output from the PPT.

(2) Disconnect power and insert the AI-1 card into the junction box. This card provides an alternating +5.0 and zero volts input to the analog MOSFET switches. Reapply power.

(3) Set the PPT as follows:

(a) Ext/Int Clock - Set Int
(b) Man/Auto Mode - Set Auto

(c) Ext/Int Strobe - Set Int
(d) Ovrd/Norm Strobe - Set Norm
(e) Auto Start Channel, 0001110 (Channel 56)
(f) Auto Stop Channel (N-1), 0010001 (Channel 68)
(g) Auto Stop Channel Override Inactive

(4) Monitor the waveform on the oscilloscope and compare with Figure 81(a). There should be 12 channel ON periods alternating +5.0 and +1.0 volt levels. The OFF periods should be zero volts. A +5.0 volt synchronization signal should identify each frame. Each frame should occupy 14 channel positions and approximately 15.5 milliseconds of time.

	-35°C	+25°C	+95°C
Operates Properly			
LO (+22) volts input	✓	✓	✓
NORM(+28) volts input	✓	✓	✓
HI (+32) volts input	✓	✓	✓

5.5.2.2 Synchronization - The amplitude of the synchronization pulse is assumed to be equal to the full scale voltage measured in 5.5.2.6, and will therefore not be measured in this section. (The validity of this assumption is based on the identical manner in which the two signals are derived and processed.)

(1) With the waveform monitored in 5.5.2.1(4), check the timing with Test Specification 5.4.2.

(2) Record:

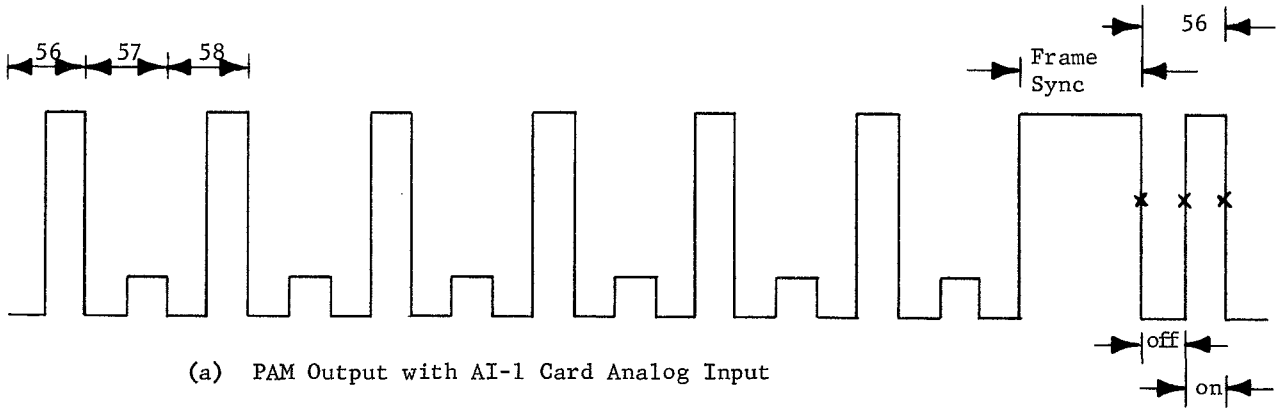
	-35°C	+25°C	+95°C
Meets Timing Specification	✓	✓	✓

5.5.2.3 Duty Cycle - Measure the OFF and ON period of Channel 56 on the oscilloscope using 50% voltage points, as shown in Figure

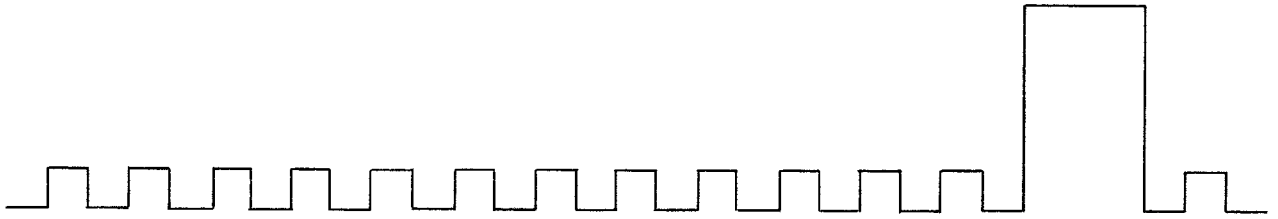
	-35°C	+25°C	+95°C
ON Period	575 µs	565 µs	560 µs
OFF Period	575 µs	565 µs	560 µs
Duty Cycle (Calculated) (See .4.3)	50%	50%	50%

5.5.2.4 Channel Period - Using the above measurements, calculate the channel period (ON period plus the OFF period).

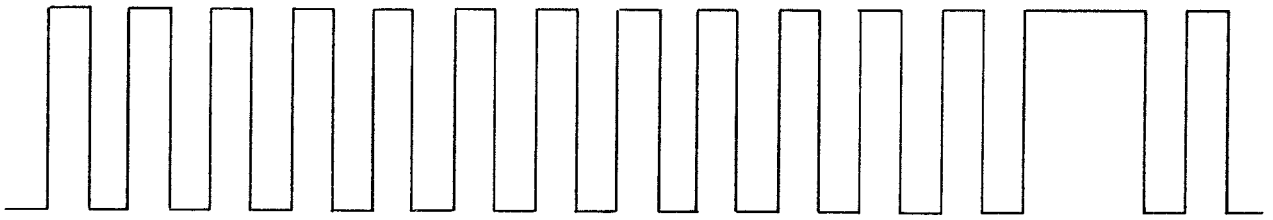
	-35°C	+25°C	+95°C
Channel Period	1150 µs	1130 µs	1120 µs



(a) PAM Output with AI-1 Card Analog Input



(b) PAM Output with AI-4 Card Analog Input (All Inputs Zero Volts)



(c) PAM Output with AI-4 Card Analog Input (All Inputs +5 Volts)

Figure 81. PAM Output General Waveform

5.5.2.5 Zero Data Pedestal

(1) Disconnect power. Insert the analog input card AI-4 into the junction box and jumper the AI-4 card for zero inputs. Reapply power.

(2) Connect scope input to PAM output and verify that waveform is as shown in Figure 81(b).

(3) Connect the digital voltmeter to the PAM output.

(4) Set the PPT as follows:

(a) Man/Auto Mode - Set Man
(b) Manual Entry - Select Channels 56 thru 67
(c) Ovrd/Norm Strobe - Set Ovrd

(5) Measure and record reading on digital voltmeter.

Output Voltage

Channel	-35°C Input Voltage			+25°C Input Voltage			+95°C Input Voltage		
	+22	+28	+32	+22	+28	+32	+22	+28	+32
56	1.018	1.018	1.019	1.019	1.020	1.020	1.027	1.028	1.028
57	1.017	1.018	1.019	1.019	1.020	1.020	1.027	1.027	1.028
58	1.017	1.018	1.018	1.019	1.019	1.020	1.027	1.027	1.028
59	1.018	1.018	1.019	1.018	1.019	1.019	1.027	1.027	1.027
60	1.018	1.018	1.018	1.019	1.019	1.019	1.027	1.027	1.027
61	1.018	1.019	1.018	1.019	1.019	1.019	1.026	1.027	1.027
62	1.017	1.017	1.017	1.019	1.019	1.019	1.027	1.027	1.027
63	1.017	1.018	1.018	1.018	1.019	1.019	1.026	1.027	1.028
64	1.018	1.019	1.019	1.019	1.019	1.020	1.026	1.027	1.027
65	1.017	1.018	1.018	1.018	1.019	1.019	1.026	1.027	1.027
66	1.016	1.019	1.018	1.018	1.019	1.019	1.026	1.027	1.027
67	1.016	1.017	1.019	1.019	1.019	1.019	1.026	1.026	1.027

5.5.2.6 Full Scale Output Amplitude

(1) Disconnect power. Change the jumper on the AI-4 card from the zero potential to the +5 volt potential. Reapply power.

(2) Set PPT as follows:

(a) Man/Auto Mode - Set Auto
(b) Ovrd/Norm Strobe - Set Norm
(c) Auto Start Channel - 0001110 (Channel 56)
(d) Auto Stop Channel (N-1), 0010001 (Channel 68)
(e) Auto Stop Channel Override Inactive (Down)

(3) Connect scope input to PAM output and verify that wavefore is as shown in Figure 81(c).

(4) Set the PPT as follows:

(a) Man/Auto Mode - Set Man
(b) Manual Entry - Select Channels 56 thru 67
(c) Ovrd/Norm Strobe - Set Ovrd

(5) Measure the +5 volt input reference with the digital voltmeter on the IA-4 card.

	-35°C			+25°C			+95°C		
	Input Voltage			Input Voltage			Input Voltage		
	+22	+28	+32	+22	+28	+32	+22	+28	+32
Reference Voltage	5.001	5.001	5.001	4.994	4.994	4.994	4.983	4.984	4.985

(6) Disconnect the scope input and connect the digital voltmeter to the PAM output.

(7) Set the PPT manual entry to select Channels 56 thru 67.

(8) Measure and record the digital voltmeter reading.

Output Error

	-35°C			+25°C			+95°C		
	Input Voltage			Input Voltage			Input Voltage		
Channel	+22	+28	+32	+22	+28	+32	+22	+28	+32
56	5.010	5.010	5.010	5.003	5.003	5.003	4.992	4.991	4.992
57	5.009	5.010	5.011	5.003	5.003	5.004	4.991	4.991	4.991
58	5.009	5.010	5.011	5.002	5.003	5.004	4.991	4.992	4.992
59	5.009	5.010	5.012	5.002	5.003	5.004	4.991	4.991	4.991
60	5.011	5.011	5.010	5.003	5.003	5.003	4.991	4.992	4.992
61	5.010	5.009	5.012	5.002	5.003	5.003	4.991	4.991	4.991
62	5.010	5.010	5.011	5.003	5.003	5.003	4.991	4.991	4.992
63	5.011	5.010	5.011	5.003	5.003	5.003	4.990	4.991	4.991
64	5.010	5.011	5.012	5.003	5.004	5.004	4.991	4.992	4.992
65	5.011	5.011	5.012	5.003	5.004	5.004	4.991	4.992	4.992
66	5.010	5.010	5.011	5.003	5.004	5.004	4.991	4.992	4.992
67	5.010	5.010	5.011	5.003	5.004	5.004	4.991	4.992	4.992

5.5.2.7 Ripple and Crosstalk

(1) Disconnect power. Insert the analog input card AI-2 into the junction box and ground Channel 56 input. Reapply power.

(2) Connect the sine wave signal generator to Channel 57 input.

(3) Set the signal generator for 1 kHz and 5 volts peak-to-peak amplitude.

(4) Set the PPT Manual Entry to Channel 56 and Strobe Ovrd/Norm to Norm.

(5) Connect scope input to PAM output and measure the total (1 kc crosstalk plus white noise) peak-to-peak noise on Channel 56.

	-35°C	+25°C	+95°C
Noise	< 20mv	< 20mv	< 20mv

5.5.2.8 OFF Time Voltage

(1) Connect the digital voltmeter to the PAM output.

(2) Disconnect power. Insert the analog input card AI-4 into the junction box with all inputs bussed to +5 volts. Reapply power.

(3) Set the PPT as follows:

(a) Man/Auto - Set Man
(b) Manual Entry Channel, 0001110 (Channel 56), Auto Stop Ovrd to Active (UP)
(c) Strobe Ext/Int - Set to Ext
(d) Strobe Ovrd/Norm - Set to Norm

(4) Connect a jumper cable between GND and Strobe Ext Input jacks on PPT and measure and record OFF time voltage at PAM output.

	OFF Voltage		
Channel	-35°C	+25°C	+95°C
56	15mv	14mv	17mv
57	15mv	15mv	17mv
58	15mv	15mv	17mv
59	15mv	14mv	17mv
60	15mv	15mv	17mv
61	15mv	14mv	17mv
62	15mv	14mv	17mv
63	15mv	14mv	16mv
64	16mv	15mv	18mv
65	16mv	15mv	17mv
66	16mv	15mv	18mv
67	16mv	15mv	17mv

5.5.3 Transducer Power

This portion of the test procedure checks the amplitude and timing of the gated transducer power, thereby verifying compliance with Test Specification 10. The analog voltage accuracies shall be monitored on a DC basis to simplify measurements. The junction box, as shown in Figures 80 and 82, will be used to monitor the gated regulator outputs. Measurements are taken at junction box terminals. Figure 83 shows the back of the card cage to facilitate making measurements at room temperature without the junction box.

5.5.3.1 For DC Voltage and Noise Measurements

(1) Set the PPT for Manual Mode (UP).

(2) Connect the digital voltmeter and oscilloscope to the junction box transducer power output labeled "GTR+" and "GTR-".

(3) Select each channel, one at a time, on PPT manual entry and junction box, correspondingly.

(4) Measure DC voltage and peak-to-peak noise. Note that the 350 ohm load is connected internally.

(5) Record measurements of all 12 channels on included data sheet.

5.5.3.2 Rise Time and ON-OFF Period Measurements

(1) Set the PPT for Automatic Mode (DOWN)

(2) Disconnect the digital voltmeter.

(3) Disconnect power. Insert the stairstep analog input card AI-3. Reapply power.

(4) Set the PPT for full 12 channel sequence.

(5) With the oscilloscope, measure the timing and rise time of the transducer power output of each channel, one at a time, as follows:

(a) Connect one trace of the oscilloscope dual-trace preamp to the junction box MOSFET, labeled "MOS OUT."
(b) Connect the other trace to the junction box transducer power output, labeled "GTR+."
(c) Select each channel, one at a time, on the junction box and verify the timing according to Test Specification 5.4.10.1 and Figure 79(b).

	-35°C	+25°C	+95°C
Timing OK	✓	✓	✓

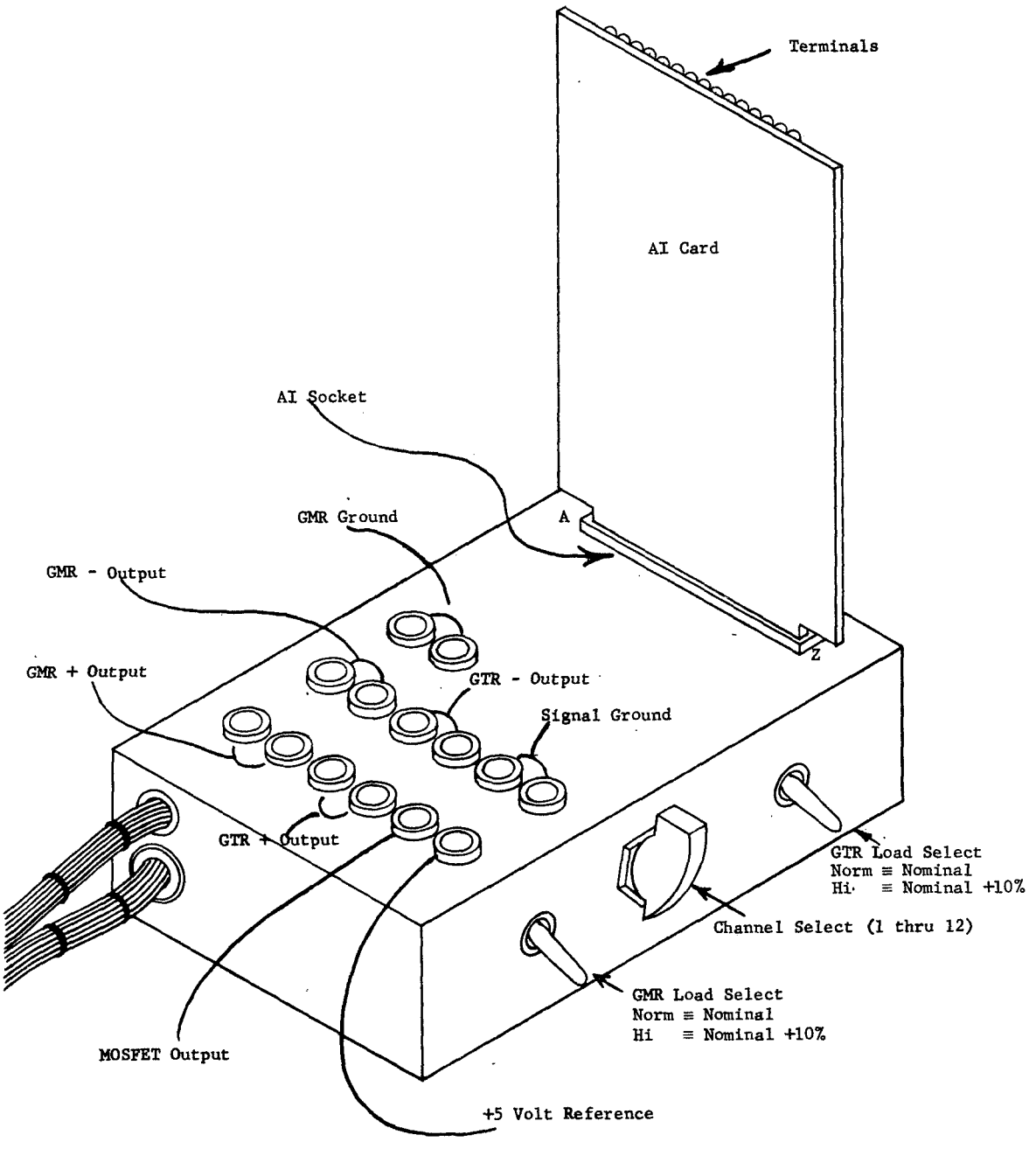
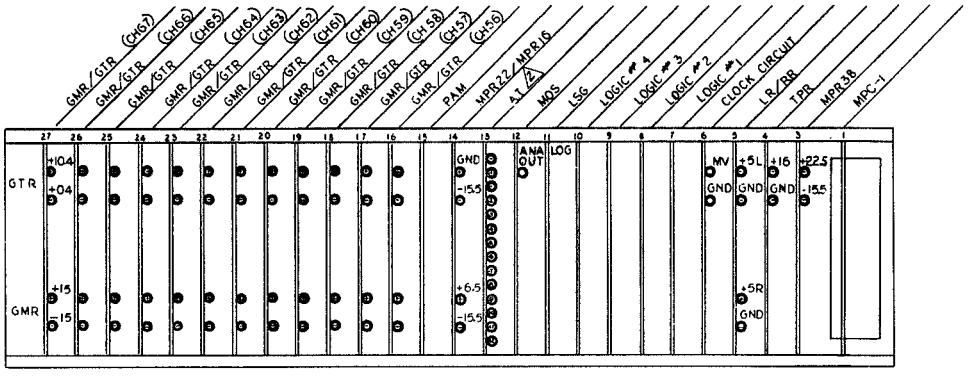


Figure 82. Junction Box



LEGEND

MPC	≡ DC TO DC CONVERTER
MPR22	≡ MODIFIER PREREGULATOR 22 VOLTS OUTPUT
MPR16	≡ MODIFIER PREREGULATOR 16 VOLTS OUTPUT
MPR38	≡ MODIFIER PREREGULATOR 38 VOLTS OUTPUT
LR	≡ LOGIC REGULATOR
RR	≡ REFRENCE REGULATOR
LSG	≡ LEVEL SHIFT GATES
MOS	≡ MOSFET MULTIPLEX SWITCHES
PAM	≡ PAM OUTPUT CIRCUIT
AI	≡ ANALOG INPUT
GMR	≡ GATED MODIFIER REGULATOR
GTR	≡ GATED TRANSDUCER REGULATOR

Figure 83. Power Programmer Breadboard
Front View of Card File

(d) Select each channel, one at a time, on the junction box and verify that the ON time, as shown in Figure 84 and the associated note, meets specification 5.4.10.2.

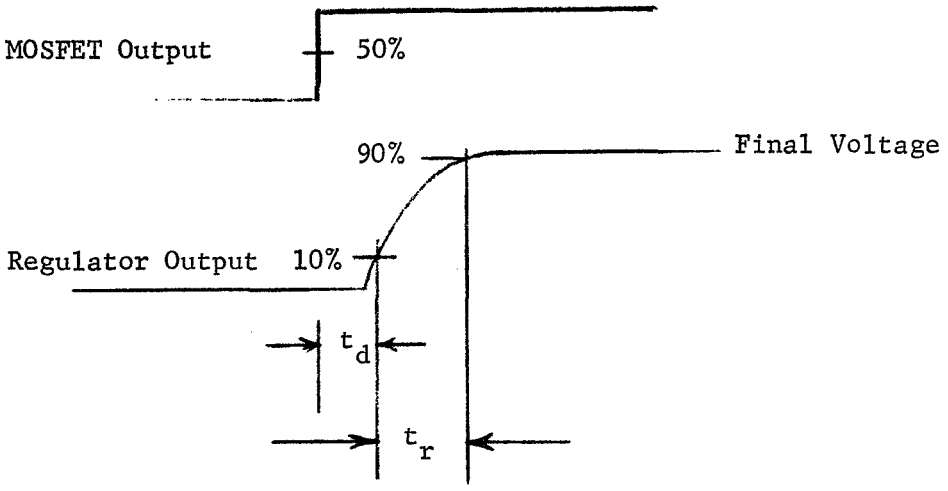


Figure 84. Regulator ON Time Measurement

NOTE: The correlation between t_r and t_r^1, where

$t_r \equiv$ 10 to 90% rise time,

$t_r^1 \equiv$ 10 to 99% rise time, is

$\frac{t_r^1}{t_r} \simeq 2.1$, assuming a single pole response (imperical information indicates the validity of this assumption).

Therefore,

$t_{ON} = t_d + t_r^1 = t_d + 2.1 \times t_r \equiv$ 99% turn ON time

Transducer Power Information

	-35°C			+25°C			+95°C		
	Input Voltage			Input Voltage			Input Voltage		
	+22	+28	+32	+22	+28	+32	+22	+28	+32
Channel 56									
Output Voltage	10.004	10.005	10.004	10.004	10.004	10.004	10.005	10.005	10.005
Noise (p to p)	<20	<20	<20	<15	<15	<15	<20	<20	<20
*t_{ON}	✓	✓	✓	✓	✓	✓	✓	✓	✓
Channel 57									
Output Voltage	10.022	10.021	10.022	10.013	10.013	10.013	10.001	10.001	10.002
Noise (p to p)	<20	<20	<20	<15	<15	<15	<20	<20	<20
*t_{ON}	✓	✓	✓	✓	✓	✓	✓	✓	✓
Channel 58									
Output Voltage	9.992	9.994	9.993	10.011	10.011	10.011	10.017	10.016	10.015
Noise (p to p)	<20	<20	<20	<15	<15	<15	<15	<15	<15
*t_{ON}	✓	✓	✓	✓	✓	✓	✓	✓	✓
Channel 59									
Output Voltage	10.014	10.015	10.013	10.016	10.016	10.016	10.018	10.018	10.019
Noise (p to p)	<20	<20	<20	<15	<15	<15	<20	<20	<20
*t_{ON}	✓	✓	✓	✓	✓	✓	✓	✓	✓
Channel 60									
Output Voltage	10.034	10.033	10.033	10.037	10.037	10.037	10.023	10.021	10.021
Noise (p to p)	<20	<20	<20	<20	<20	<20	<20	<20	<20
*t_{ON}	✓	✓	✓	✓	✓	✓	✓	✓	✓
Channel 61									
Output Voltage	10.000	10.000	10.000	9.994	9.993	9.993	10.003	10.003	10.004
Noise (p to p)	<20	<20	<20	<15	<15	<15	<20	<20	<20
*t_{ON}	✓	✓	✓	✓	✓	✓	✓	✓	✓
Channel 62									
Output Voltage	10.011	10.012	10.012	10.003	10.003	10.003	10.014	10.013	10.013
Noise (p to p)	<20	<20	<20	<20	<20	<20	<20	<20	<20
*t_{ON}	✓	✓	✓	✓	✓	✓	✓	✓	✓
Channel 63									
Output Voltage	10.004	10.002	10.003	9.991	9.990	9.990	10.002	10.002	10.002
Noise (p to p)	<20	<20	<20	<15	<15	<15	<20	<20	<20
*t_{ON}	✓	✓	✓	✓	✓	✓	✓	✓	✓
Channel 64									
Output Voltage	10.000	10.000	10.000	10.015	10.015	10.015	9.998	9.997	9.997
Noise (p to p)	<25	<25	<25	<20	<20	<20	<20	<20	<20
*t_{ON}	✓	✓	✓	✓	✓	✓	✓	✓	✓

*See Figure 8 and associated Note.

Transducer Power Information

	-35°C			+25°C			+95°C		
	Input Voltage			Input Voltage			Input Voltage		
	+22	+28	+32	+22	+28	+32	+22	+28	+32
Channel 65									
Output Voltage	10.002	10.003	10.003	9.976	9.974	9.975	10.001	10.001	10.001
Noise (p to p)	<20	<20	<20	<20	<20	<20	<20	<20	<20
*t_{ON}	✓	✓	✓	✓	✓	✓	✓	✓	✓
Channel 66									
Output Voltage	10.014	10.014	10.015	10.014	10.014	10.014	10.005	10.005	10.005
Noise (p to p)	<20	<20	<20	<15	<15	<15	<15	<15	<15
*t_{ON}	✓	✓	✓	✓	✓	✓	✓	✓	✓
Channel 67									
Output Voltage	9.994	9.994	9.994	10.013	10.013	10.013	9.998	9.998	9.999
Noise (p to p)	<20	<20	<20	<15	<15	<15	<15	<15	<15
*t_{ON}	✓	✓	✓	✓	✓	✓	✓	✓	✓

*See Figure 84 and associated Note.

5.5.4 Signal Modifier Power

This portion of the test procedure checks the amplitude and timing of the gated modifier power, thereby verifying compliance with Test Specification 11. The analog voltage accuracies shall be monitored on a DC basis to simplify measurements. The junction box as shown in Figures 80 and 82 will be used to monitor the gated regulator outputs.

5.5.4.1 DC Voltage and Noise Measurements

(1) Set the PPT for Manual Mode (UP).

(2) Connect the digital voltmeter and oscilloscope to the junction box signal modifier power output labeled "GMR+" and "GMR-."

(3) Select each channel, one at a time, on PPT manual entry and junction box, correspondingly.

(4) Measure DC voltage and peak-to-peak noise. Note that the 6 ma load is connected internally.

(5) Record measurements of all 12 channels on included data sheet.

5.5.4.2 Rise Time and ON-OFF Period Measurements

(1) Set the PPT for Automatic Mode (DOWN).

(2) Disconnect the digital voltmeter.

(3) Disconnect power. Insert the stairstep analog input card AI-3. Reapply power.

(4) Set the PPT for full 12 channel sequence.

(5) Measure with the oscilloscope the timing and rise time of both the positive and negative signal modifier outputs of each channel, one at a time, as follows:

(a) Connect one trace of the oscilloscope dual-trace preamp to the junction box MOSFET outputs labeled "MOS OUT."

(b) Connect the other trace to the junction box signal modifier output labeled "GMR+" and "GMR-."

(c) Select each channel, one at a time, on the junction box and verify the timing according to Test Specification 5.4.11.1 and Figure 79(b).

	-35°C	+25°C	+95°C
Timing OK	✓	✓	✓

(d) Select each channel, one at a time, on the junction box and verify that the ON time, as shown in Figure 84 and the associated Note, meet Test Specification 5.4.11.2.

Signal Modifier Power Information

	-35°C			+25°C			+95°C		
	Input Voltage			Input Voltage			Input Voltage		
	+22	+28	+32	+22	+28	+32	+22	+28	+32
Channel 56									
Output Voltage (differential)	29.994	29.995	29.995	29.978	29.977	29.977	30.088	30.260	30.310
Noise (p to p)	<20	<20	<20	<20	<20	<20	<20	<20	<20
*t_{ON} Positive Output	✓	✓	✓	✓	✓	✓	✓	✓	✓
*t_{ON} Negative Output	✓	✓	✓	✓	✓	✓	✓	✓	✓
Channel 57									
Output Voltage (differential)	30.005	30.005	30.005	30.046	30.046	30.046	30.119	30.181	30.233
Noise (p to p)	<20	<20	<20	<20	<20	<20	<20	<20	<20
*t_{ON} Positive Output	✓	✓	✓	✓	✓	✓	✓	✓	✓
*t_{ON} Negative Output	✓	✓	✓	✓	✓	✓	✓	✓	✓

*See Figure 84 and Associated Note

Signal Modifier Power Information

	-35°C			+25°C			+95°C		
	Input Voltage			Input Voltage			Input Voltage		
	+22	+28	+32	+22	+28	+32	+22	+28	+32
Channel 58									
Output Voltage (differential)	30.024	30.024	30.025	30.096	30.096	30.096	30.138	30.223	30.244
Noise (p to p)	<20	<20	<20	<20	<20	<20	<20	<20	<20
*t_{ON} Positive Output	✓	✓	✓	✓	✓	✓	✓	✓	✓
*t_{ON} Negative Output	✓	✓	✓	✓	✓	✓	✓	✓	✓
Channel 59									
Output Voltage (differential)	30.079	30.079	30.079	30.026	30.026	30.026	29.987	30.048	30.069
Noise (p to p)	<20	<20	<20	<20	<20	<20	<20	<20	<20
*t_{ON} Positive Output	✓	✓	✓	✓	✓	✓	✓	✓	✓
*t_{ON} Negative Output	✓	✓	✓	✓	✓	✓	✓	✓	✓
Channel 60									
Output Voltage (differential)	30.051	30.052	30.052	30.034	30.034	30.034	29.999	30.084	30.110
Noise (p to p)	<20	<20	<20	<20	<20	<20	<20	<20	<20
*t_{ON} Positive Output	✓	✓	✓	✓	✓	✓	✓	✓	✓
*t_{ON} Negative Output	✓	✓	✓	✓	✓	✓	✓	✓	✓
Channel 61									
Output Voltage (differential)	30.120	30.120	30.120	30.045	30.045	30.045	30.058	30.139	30.170
Noise (p to p)	<20	<20	<20	<20	<20	<20	<20	<20	<20
*t_{ON} Positive Output	✓	✓	✓	✓	✓	✓	✓	✓	✓
*t_{ON} Negative Output	✓	✓	✓	✓	✓	✓	✓	✓	✓
Channel 62									
Output Voltage (differential)	30.095	30.095	30.095	30.047	30.047	30.42	29.981	30.024	30.041
Noise (p to p)	<20	<20	<20	<20	<20	<20	<20	<20	<20
*t_{ON} Positive Output	✓	✓	✓	✓	✓	✓	✓	✓	✓
*t_{ON} Negative Output	✓	✓	✓	✓	✓	✓	✓	✓	✓

*See Figure 84 and Associated Note.

Signal Modifier Power Information

	-35°C			+25°C					
	Input Voltage			Input Voltage			Input Voltage		
	+22	+28	+32	+22	+28	+32	+22	+28	+32
Channel 63									
Output Voltage (differential)	30.100	30.100	30.099	30.061	30.064	30.061	30.128	30.211	30.252
Noise (p to p)	<20	<20	<20	<20	<20	<20	<20	<20	<20
*t_{ON} Positive Output	✓	✓	✓	✓	✓	✓	✓	✓	✓
*t_{ON} Negative Output	✓	✓	✓	✓	✓	✓	✓	✓	✓
Channel 64									
Output Voltage (differential)	30.128	30.128	30.128	30.042	30.043	30.043	29.966	30.021	30.033
Noise (p to p)	<20	<20	<20	<20	<20	<20	<20	<20	<20
*t_{ON} Positive Output	✓	✓	✓	✓	✓	✓	✓	✓	✓
*t_{ON} Negative Output	✓	✓	✓	✓	✓	✓	✓	✓	✓
Channel 65									
Output Voltage (differential)	30.110	30.110	30.111	30.034	30.034	30.034	29.881	29.886	29.886
Noise (p to p)	<20	<20	<20	<20	<20	<20	<20	<20	<20
*t_{ON} Positive Output	✓	✓	✓	✓	✓	✓	✓	✓	✓
*t_{ON} Negative Output	✓	✓	✓	✓	✓	✓	✓	✓	✓
Channel 66									
Output Voltage (differential)	30.021	30.021	30.020	30.032	30.031	30.031	29.857	29.883	29.907
Noise (p to p)	<20	<20	<20	<20	<20	<20	<20	<20	<20
*t_{ON} Positive Output	✓	✓	✓	✓	✓	✓	✓	✓	✓
*t_{ON} Negative Output	✓	✓	✓	✓	✓	✓	✓	✓	✓
Channel 67									
Output Voltage (differential)	29.945	29.945	29.946	30.011	30.015	30.016	29.912	29.949	29.957
Noise (p to p)	<20	<20	<20	<20	<20	<20	<20	<20	<20
*t_{ON} Positive Output	✓	✓	✓	✓	✓	✓	✓	✓	✓
*t_{ON} Negative Output	✓	✓	✓	✓	✓	✓	✓	✓	✓

*See Figure 84 and Associated Note.

6. CONCLUSIONS AND RECOMMENDATIONS

6.1 CONCLUSIONS

This contract successfully demonstrated the following points:

a) Contract specifications were met and in many respects exceeded.

b) The system approach is functional and offers decided advantage over existing systems with respect to power, size, and weight.

c) Monolithic integrated circuits are applicable to high precision, low level signal conditioning.

d) Advanced microelectronic techniques (cermet evaporated resistors, MOSFET, complementary bipolar, and advanced circuits) can significantly affect the system organization, thereby allowing superior system techniques to be used.

e) Power was decreased by a factor of 36 with relationship to present systems. This can further be advanced to a factor of 80. (See Section 2.4)

6.2 RECOMMENDATIONS

It is recognized that this advanced development contract has yielded a system approach which offers many advantages over existing space systems. It is therefore recommended that the continuing effort be directed toward:

Phase I: Design and fabrication of a complete 90-channel breadboard system, which includes all microminiature modules.

Phase II: Design and fabrication of a complete flight qualified microminiature 90-channel system.

In Phase I all of the circuits need to be reduced to microminiature form. The PDM and DPDM output circuits and the signal modifiers should be designed and fabricated. The power converter should be upgraded to reduce the overall system power input. Since the Power Programmer concept is primarily directed toward minimizing the input power, further attention is appropriate to increase the power efficiency of the power source. This can be accomplished by applying negative

feedback around the converter, thereby significantly improving the line-load-temperature regulation of the converter. This, in turn, would allow the removal of the series preregulators, consequently decreasing the total power input by 30 to 40 percent. The operation of all 90 channels should be demonstrated in breadboard form before the system package design is undertaken. In this way many problems can be resolved before the system is fabricated in final form.

In Phase II the system microelectronic package should be designed and fabricated. The final system should be fully tested for flight qualification.

APPENDIX A

SIGNAL MODIFIER INFORMATION

APPENDIX A

SIGNAL MODIFIER INFORMATION

The amplifier used in the family of signal modifiers is specified in Table A-1. The schematic is shown in Figure A-1. The circuit is fabricated on three die:

SCA4-1 - Basic Amplifier

SCA4-2 - Drift-Offset Control Circuit and Feedback Resistors

CAP - Rolloff Capacitors

The first two die are shown in Figures A-2 and A-3, respectively, with photographs of the SCA4-1 included in Figures A-4 and A-5. The common substrate, MCD4, used in the SCA4-1 and SCA4-2 is shown in Figure A-6. This amplifier can be assembled in one package, as shown in Figure A-7.

Measured data of output voltage offset versus temperature, open loop voltage gain versus temperature, and common mode rejection versus frequency are included in Figures A-8, A-9, and A-10 respectively.

TABLE A-I. SIGNAL CONDITIONING AMPLIFIER SPECIFICATIONS

Temperature range	$-35^{\circ}C$ to $+95^{\circ}C$
Input voltage offset	≤ 20 μv
Input voltage drift	≤ 0.5 μv/$^{\circ}C$
Input current	≤ 200 na
Input current differential	≤ 40 na
Closed loop gains	1000 ±0.1% initial setting (±0.3% over temperature range) to 50 ±0.1% initial setting (±0.1% over temperature range)
Common-mode rejection	≥ 100 db at Closed loop gain = 1000 from dc to 1 kc
Power supply rejection	≤10 μv/volt
Differential input impedance	>10 megohms*
Common-mode input impedance	>50 megohms*
Output impedance	<0.2 ohm*
Output voltage	±5 volts operating (±8 volts maximum)
Linearity	< 0.1% for above output voltage range*
Supply voltages	±15 volts
Power dissipation	150 mw
Package	3/8" x 3/8", fourteen-lead flat package

*Specified at a closed loop gain of 1000

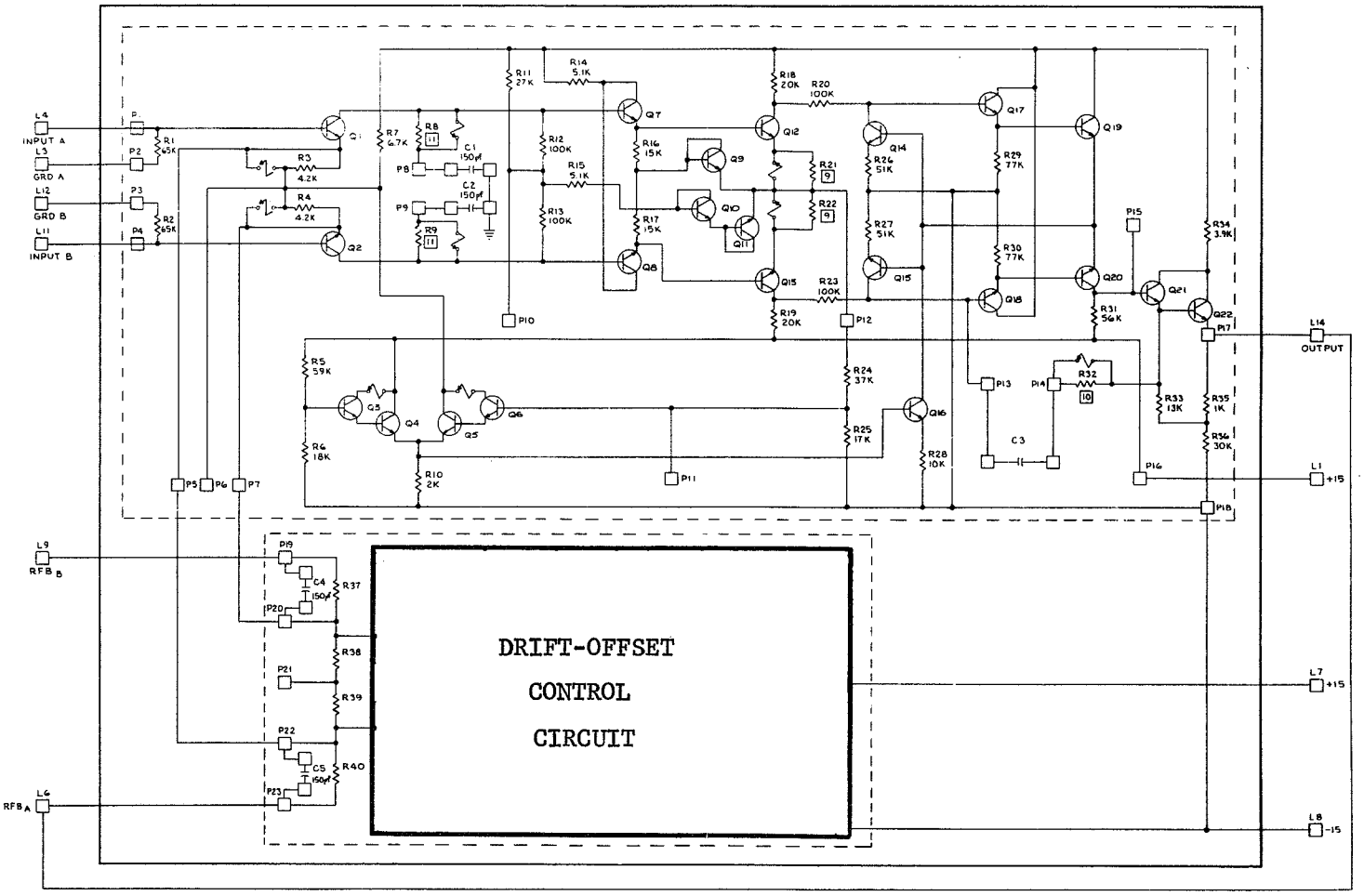


Figure A-1. Signal Conditioner Amplifier Schematic

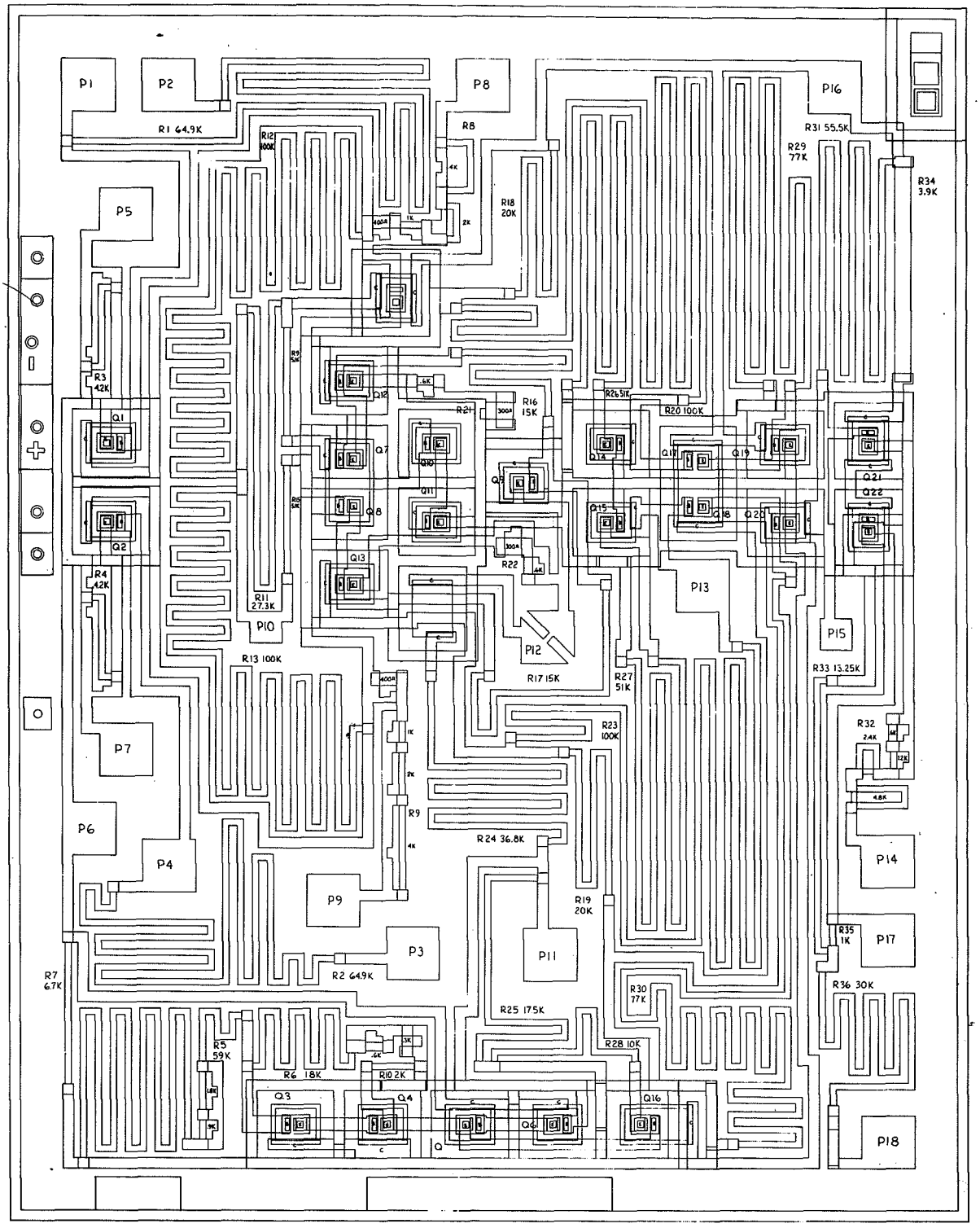


Figure A-2. Signal Conditioner Amplifier (SCA-01) Die Drawing

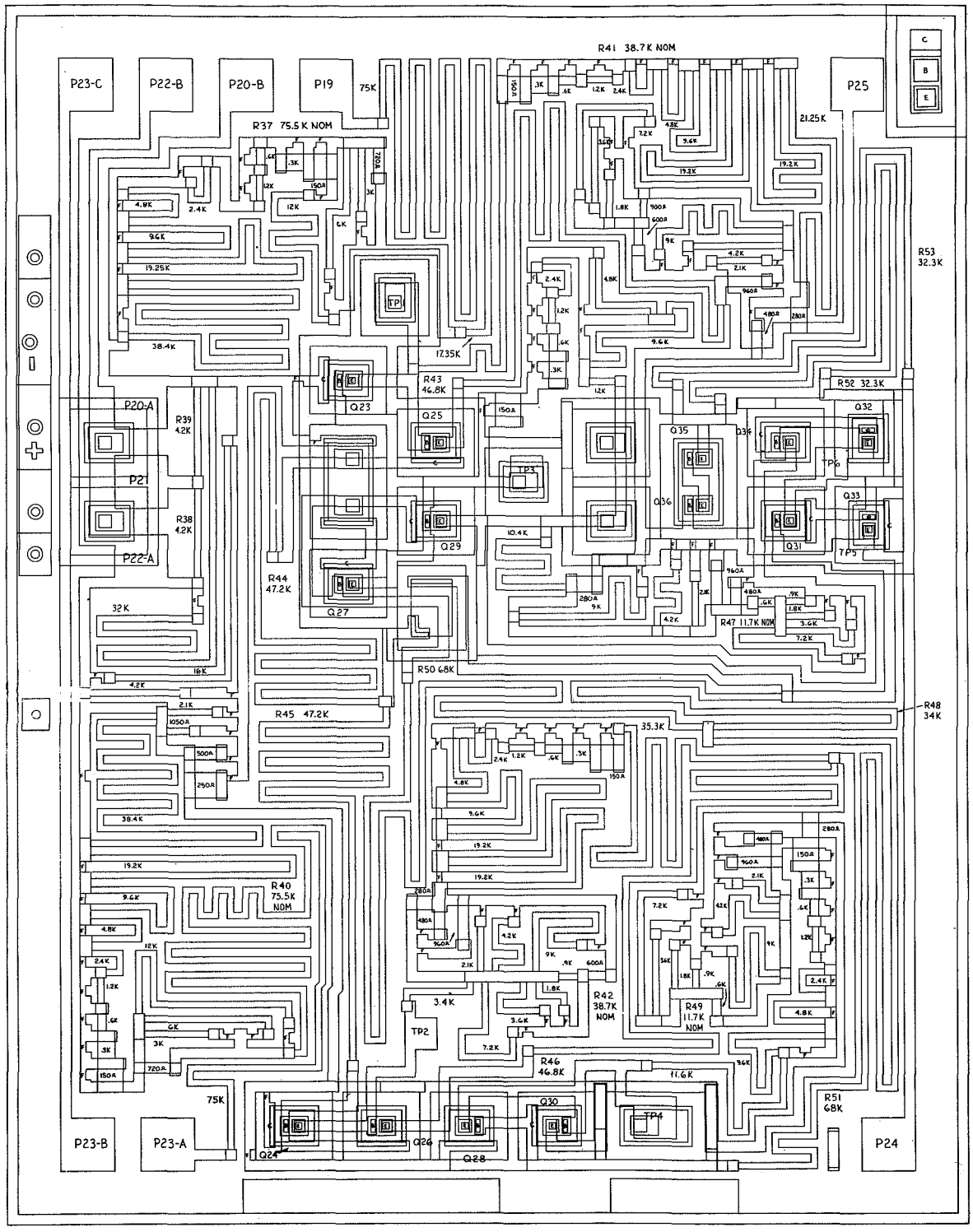


Figure A-3. Signal Conditioner Amplifier (SCA4-2) Die Drawing

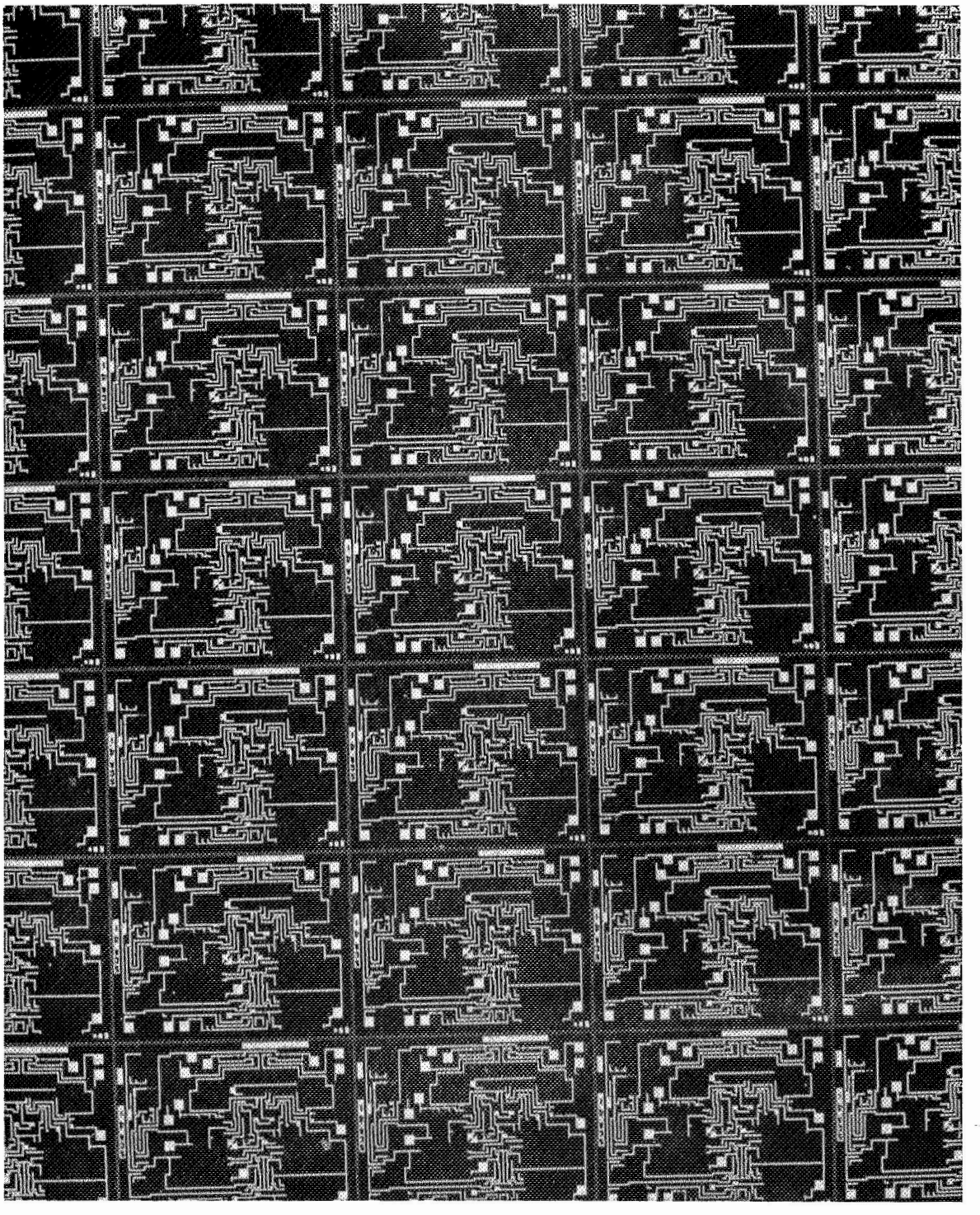


Figure A-4. Photograph of Signal Conditioner (SCA4-1) Wafer

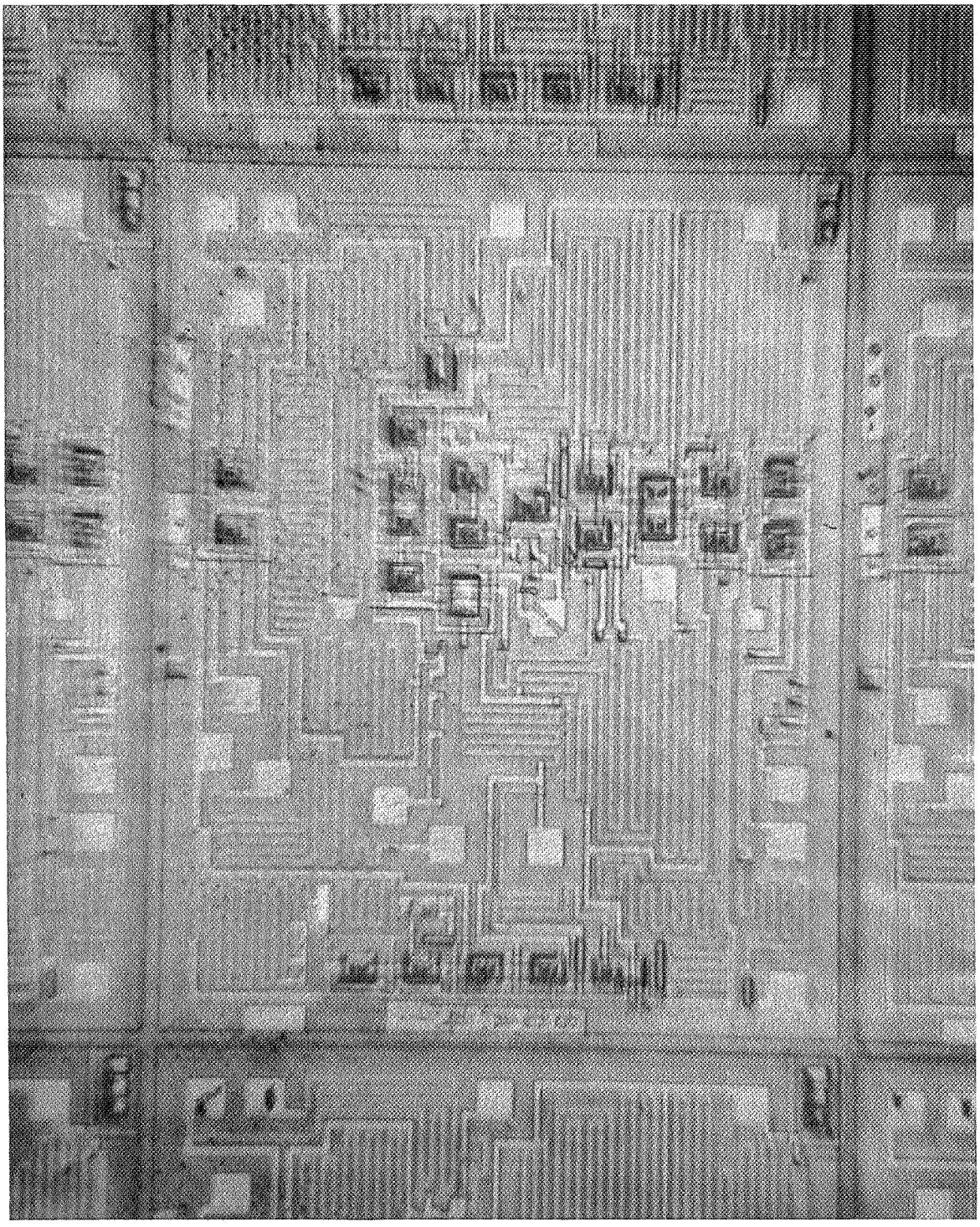


Figure A-5. Photograph of Signal Conditioner (SCA4-1) Die

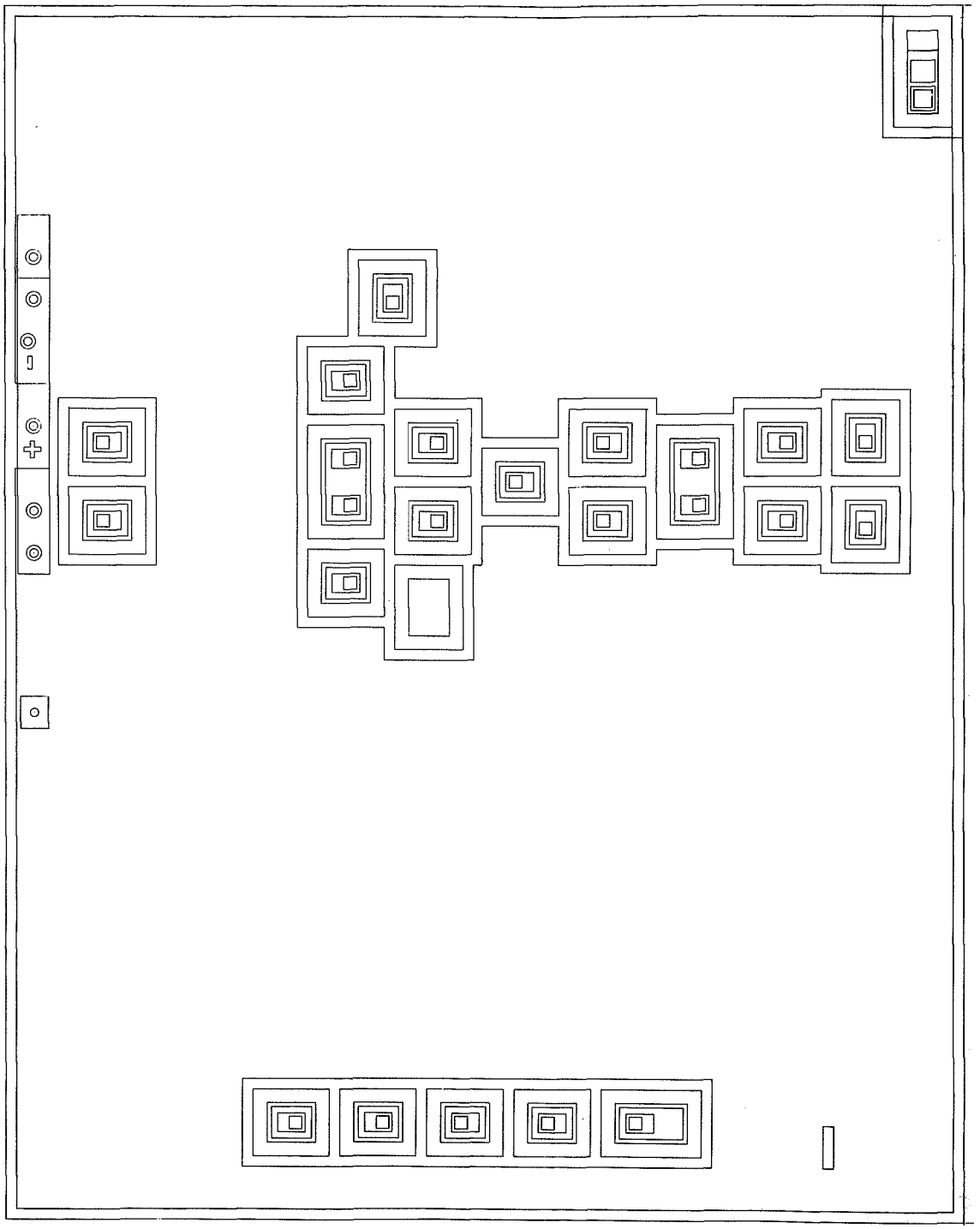


Figure A-6. Multi-Circuit Die Common Substrate (MCD4) Drawing

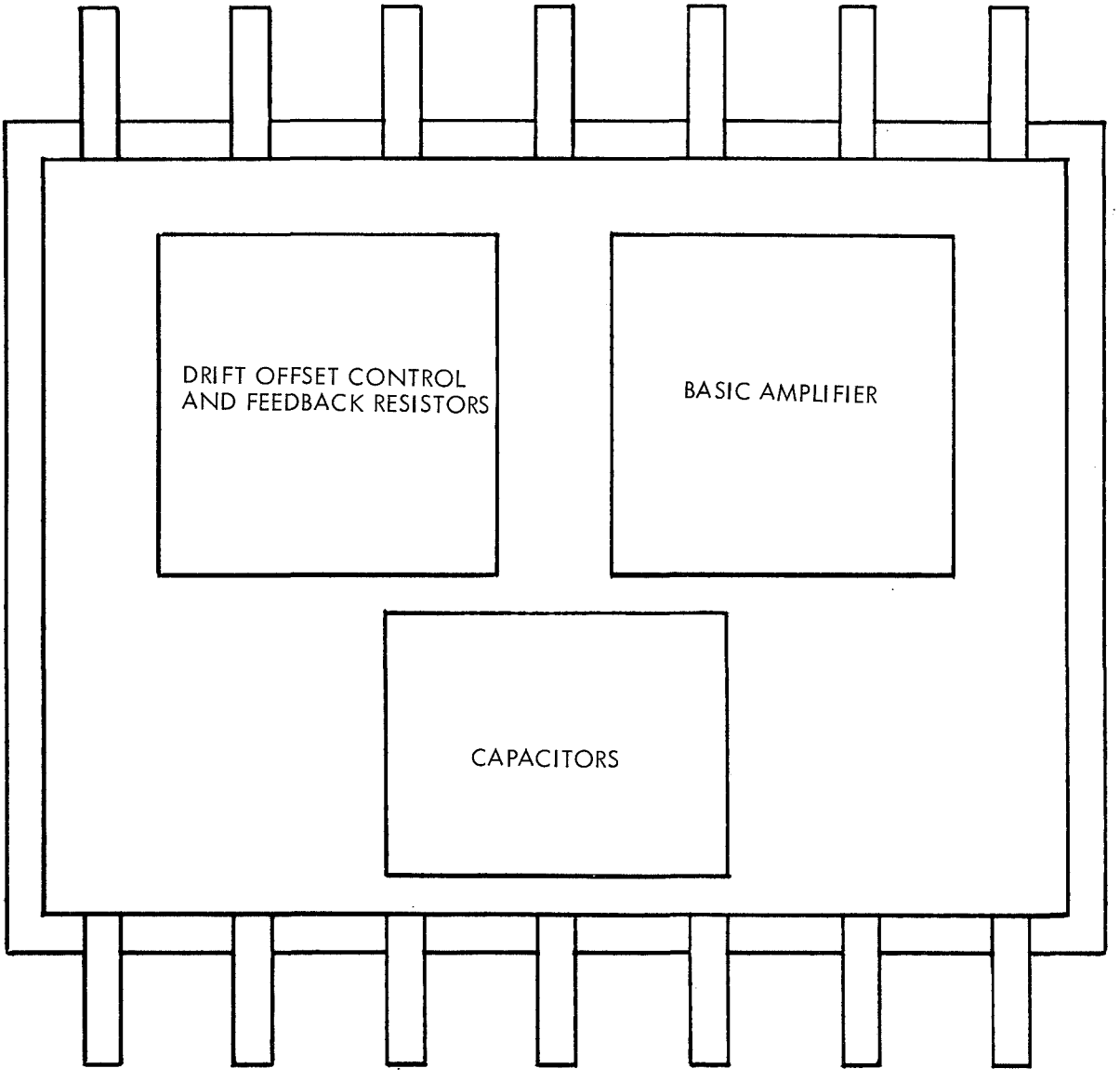


Figure A-7. Sketch of Assembled Amplifier Package

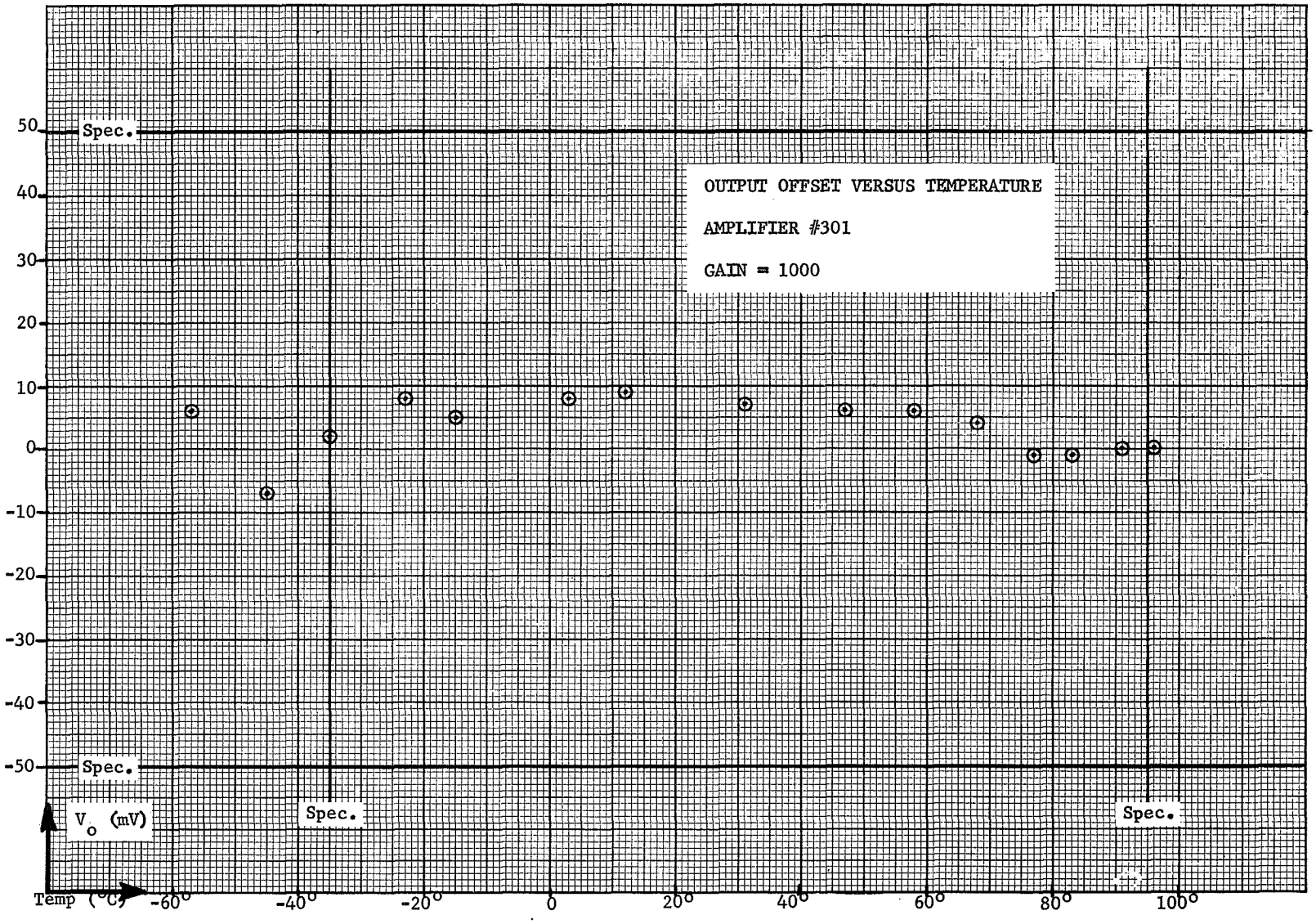


Figure A-8. Output Voltage Offset vs. Temperature Curve

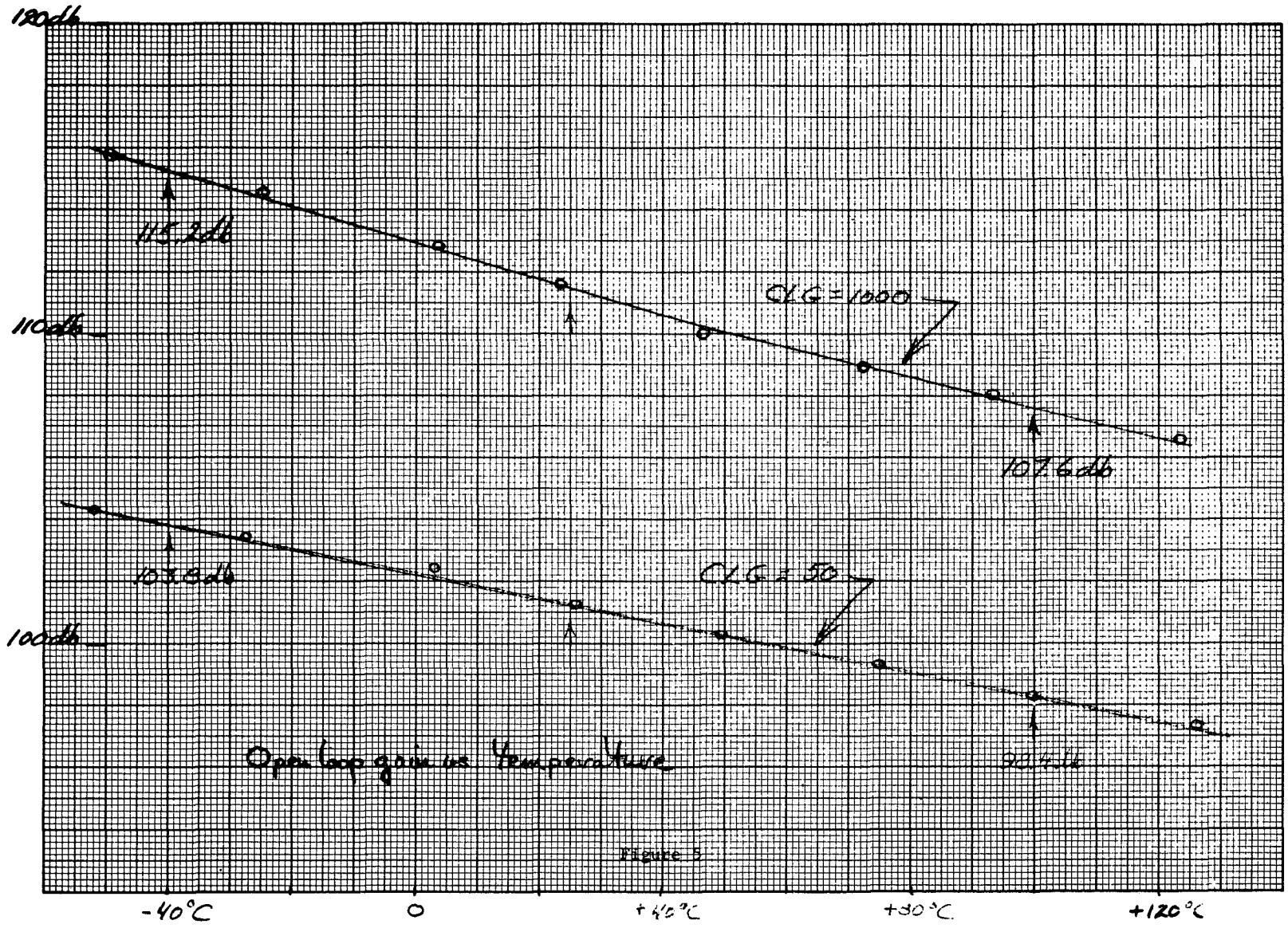


Figure A-9. Open Loop Voltage Gain vs. Temperature Curve

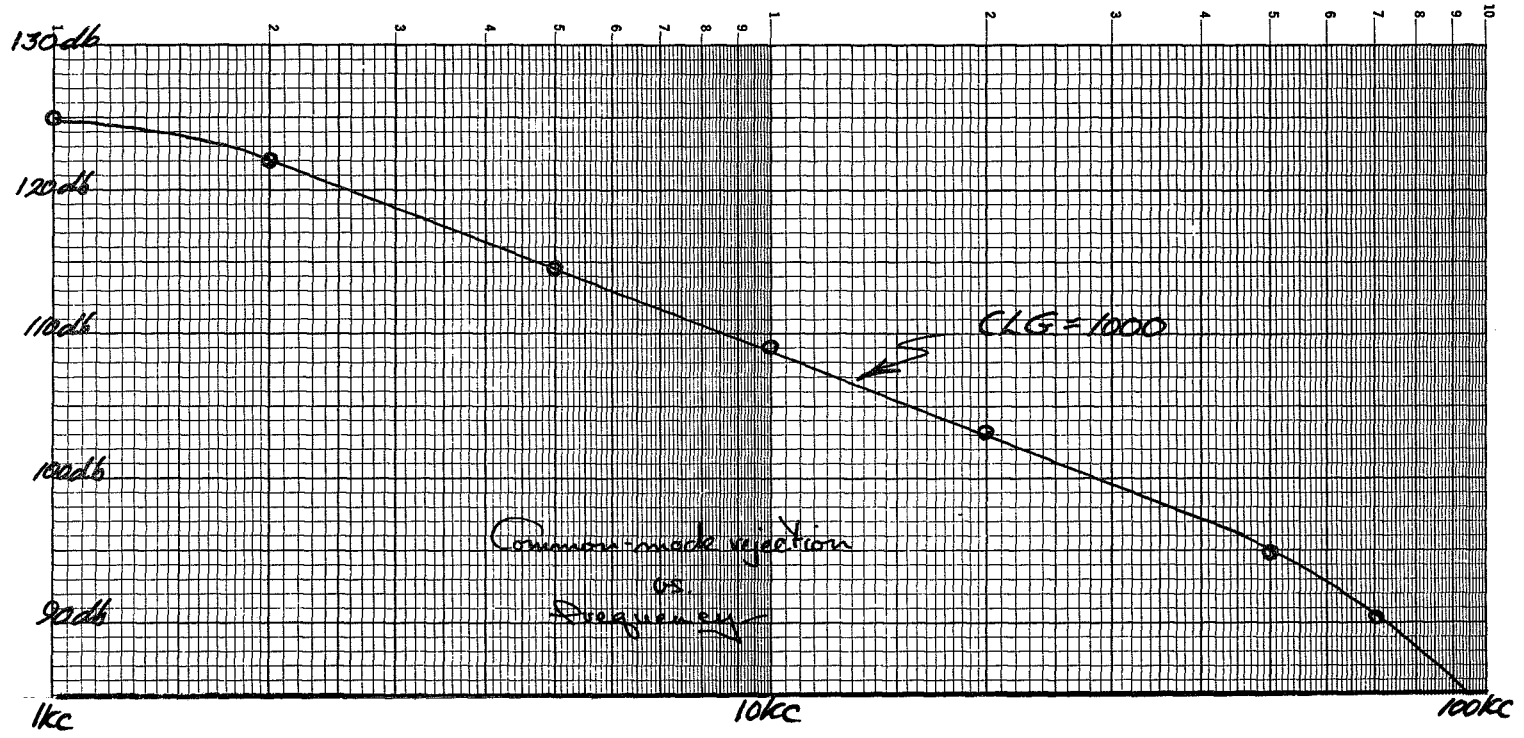


Figure A-10. Common Mode Rejection vs. Frequency Curve

APPENDIX B

SYSTEM COMPARISONS

APPENDIX B

SYSTEM COMPARISONS

Figure B-1 repeats the Power Programmer system block diagram for comparison with a "conventional" low level multiplexer analog system also shown. Table B-I lists some items of comparison. Note that the Power Programmer approach has been made realizable due to the advanced low level, direct coupled amplifier developed under NAS 9-3410 and NAS 9-4640. (Power gating chopper-stabilized amplifiers are impractical due to the typically long settling time characteristic.)

The Power Programmer can be packaged with the signal modifiers included in the main package or separately located at the sensor site, Figure B-2. Table B-II considers some of the system tradeoffs involved with those two packaging alternatives.

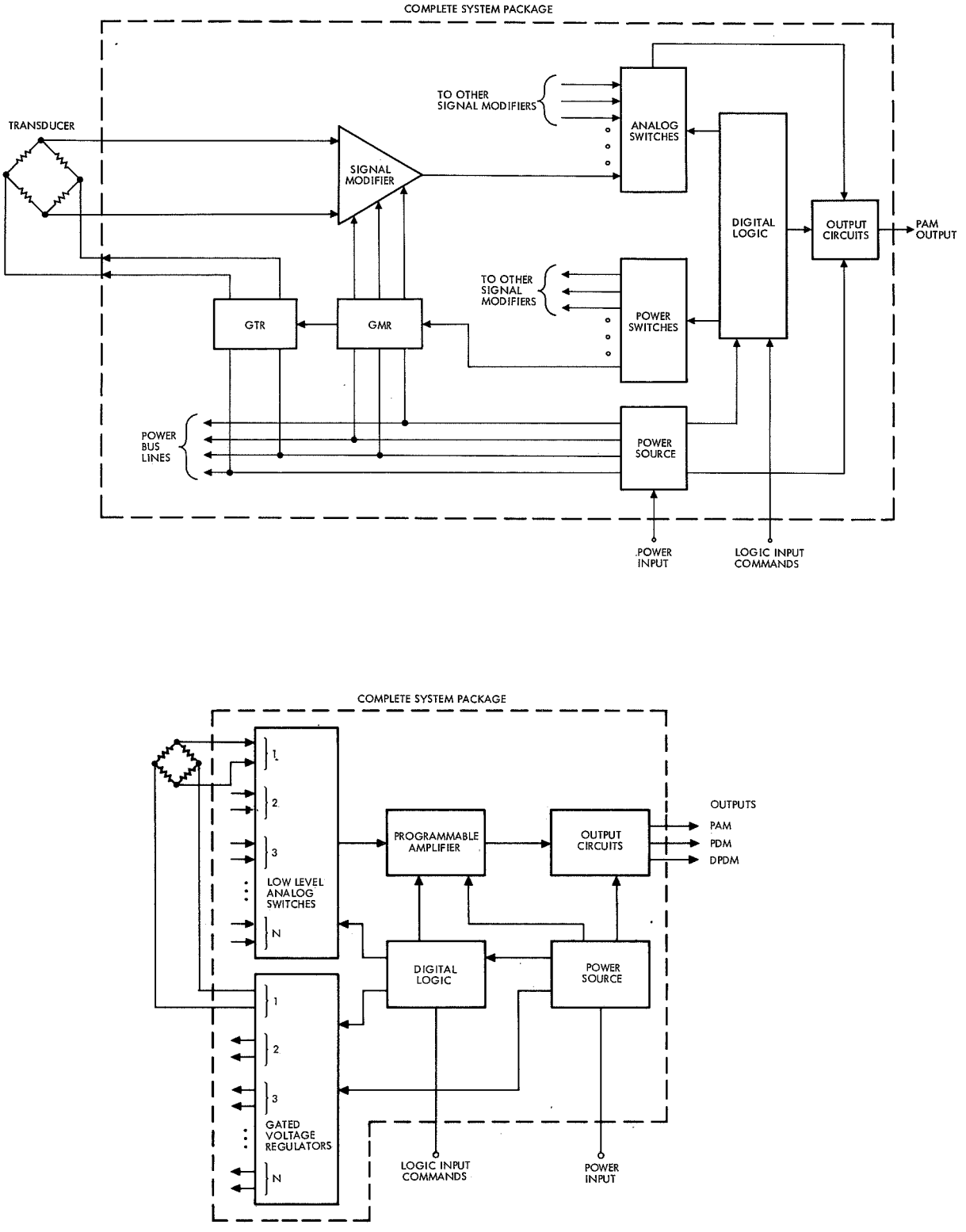


Figure B-1. Block Diagram Comparison of High Level Switching Power Programmer and Conventional Low Level Switching System

TABLE B-I. COMPARISON OF HIGH AND LOW LEVEL SWITCHING TECHNIQUES

	Separate Packaging High Level Switching System	Low Level Switching System
Universality	Complete Flexibility in choosing signal modifiers.	Signal modification limited to amplification. Amplifier gains programmed and therefore limited.
Economy	More expensive (more universal).	Less expensive (restricted application).
Analog Errors	Analog signals transferred and switched at a high level. (Smaller analog errors.)	Analog signals transferred and switched at a low level. (Larger analog errors.)
Connections	184 connections at programmer package. 6 connections at each modifier assembly.	356 connections.
Power	Same, if both systems include gated transducer power. System without gated transducers require more power.	———
Speed	Speed not limited because a channel can be turned on in advance.	Speed limited by the settling time of the amplifier.
Reliability	Not subject to catastrophic failure since 1 amp affects only 1 channel.	———

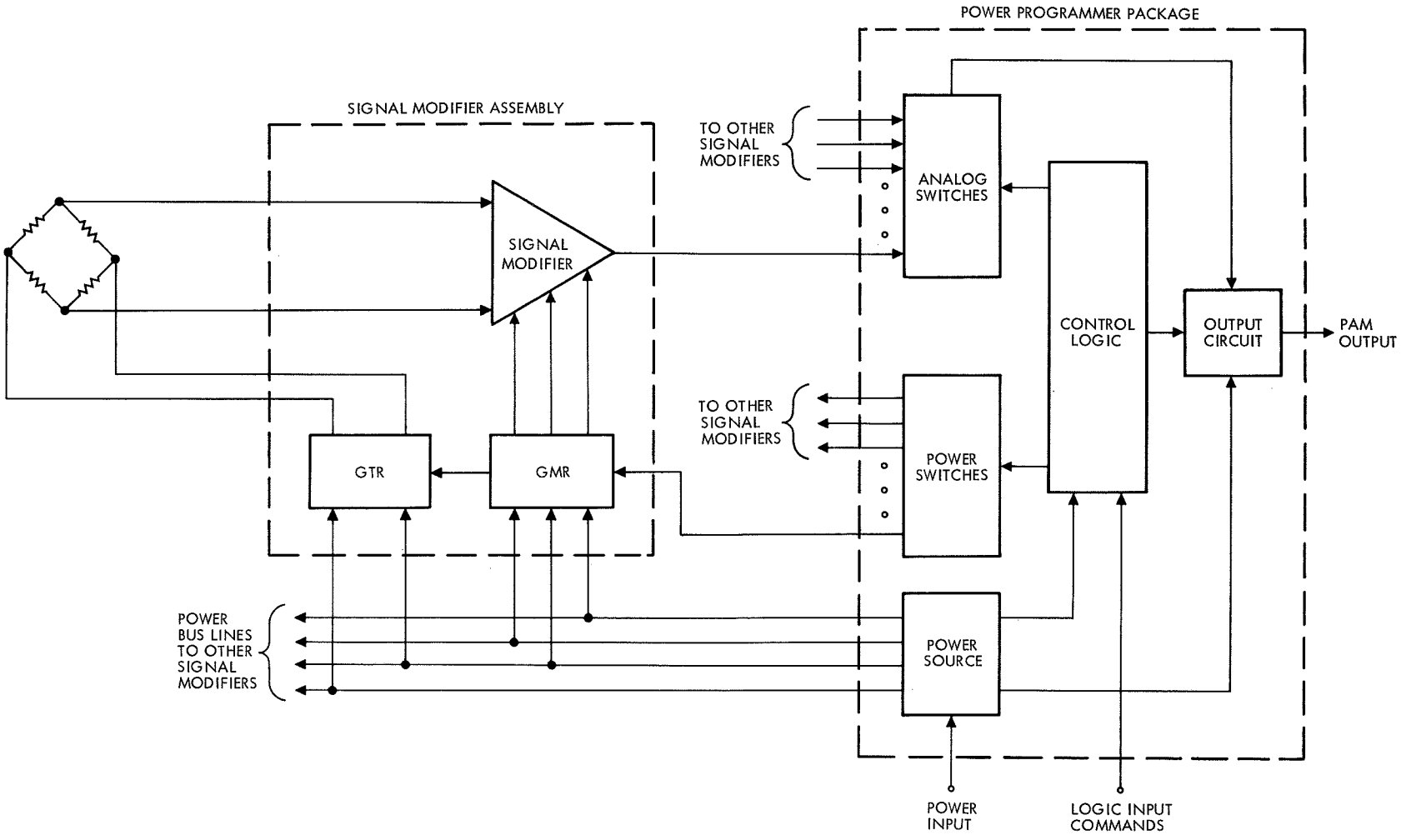


Figure B-2. Separate Package Configuration of High Level Switching

TABLE B-II. COMPARISON OF SYSTEM PACKAGING TECHNIQUES

	Separate Packaging	Single Package
Universality	Complete flexibility in choosing signal modifiers.	Signal modifiers specified and unchangeable.
Economy	Universality provides economical adaptation.	Expensive to change configuration.
	Assembly, test, and repair more economical.	Assembly, test, and repair less economical.
Analog Errors	Analog signals transferred at high level.	Analog signals transferred at low level.
Transducer Errors	Transducer power regulated at transducer.	Transducer power regulated at a distance.
Connections	184 connections at programmer package. 6 connections at each modifier assembly.	356 connections.
Volume	Programmer package smaller. Overall total volume larger.	———
Power	Same.	Same.

APPENDIX C

SYSTEM BREADBOARD INFORMATION

APPENDIX C

SYSTEM BREADBOARD INFORMATION

The following figures provide additional information on the Power Programmer Breadboard delivered under Contract No. NAS 9-5293:

Figure C-1: Power Programmer Test Unit

Figure C-2: Breadboard Under Test

Figure C-3: Card File Assembly

Figure C-4: Cabinet and Tester Assembly

Figure C-5: Card File—Card Positions

Figure C-6: Logic Diagram—Switches and Drivers

Figure C-7: Logic Diagram—Control

Figure C-8: Logic Diagram—Counter

Figure C-9: Power Distribution

Figure C-10: Analog Input Options

Figure C-11: Test Unit Indicators

Figure C-12: Junction Box Switches

Figure C-13: Junction Box Connector

Figure C-14: Test Unit Frequency Divider

Figure C-15: Test Unit Connector

Figure C-16 through C-27: Twelve Channels of Regulator Voltage versus Temperature

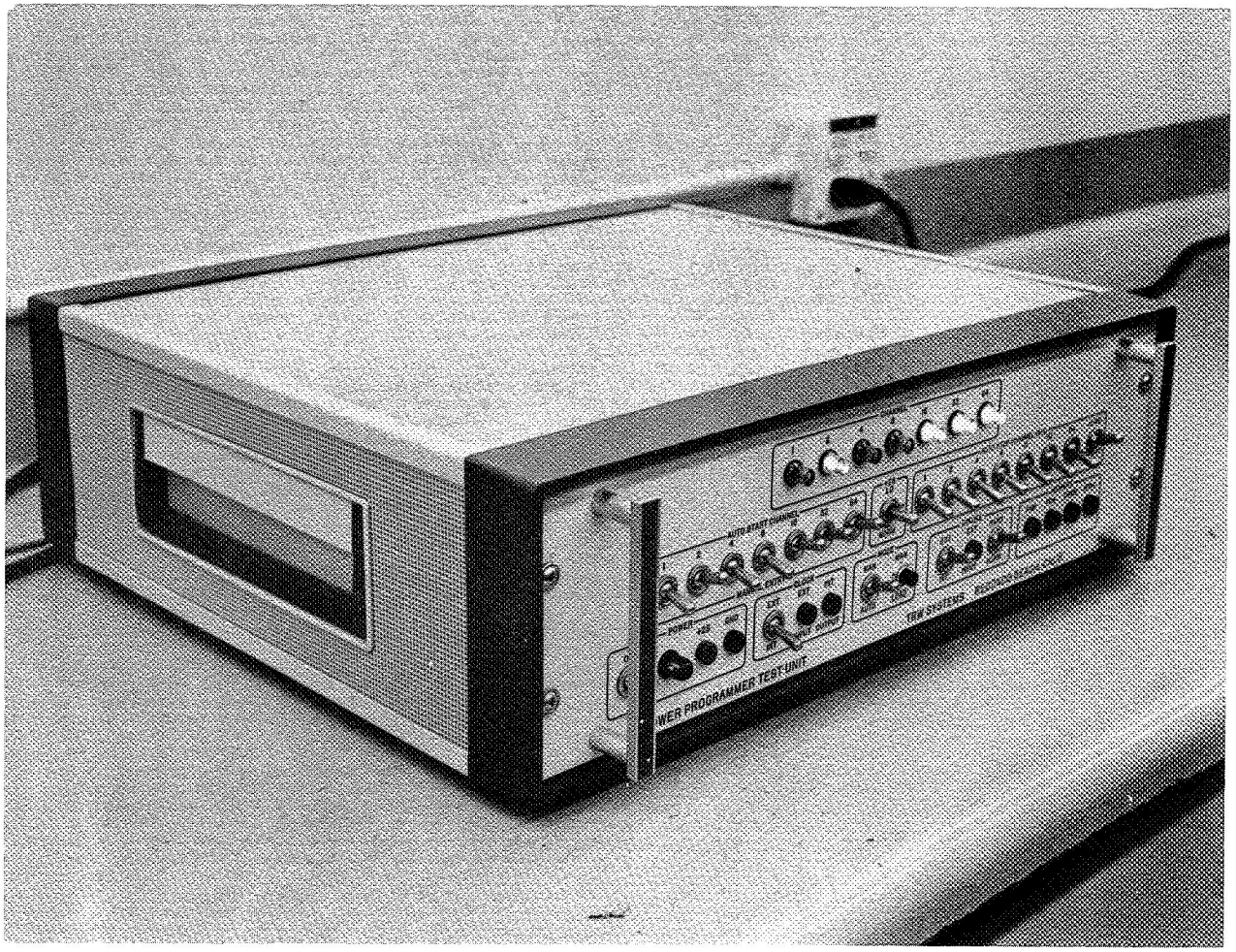


Figure C-1. Photograph of Power Programmer Test Unit

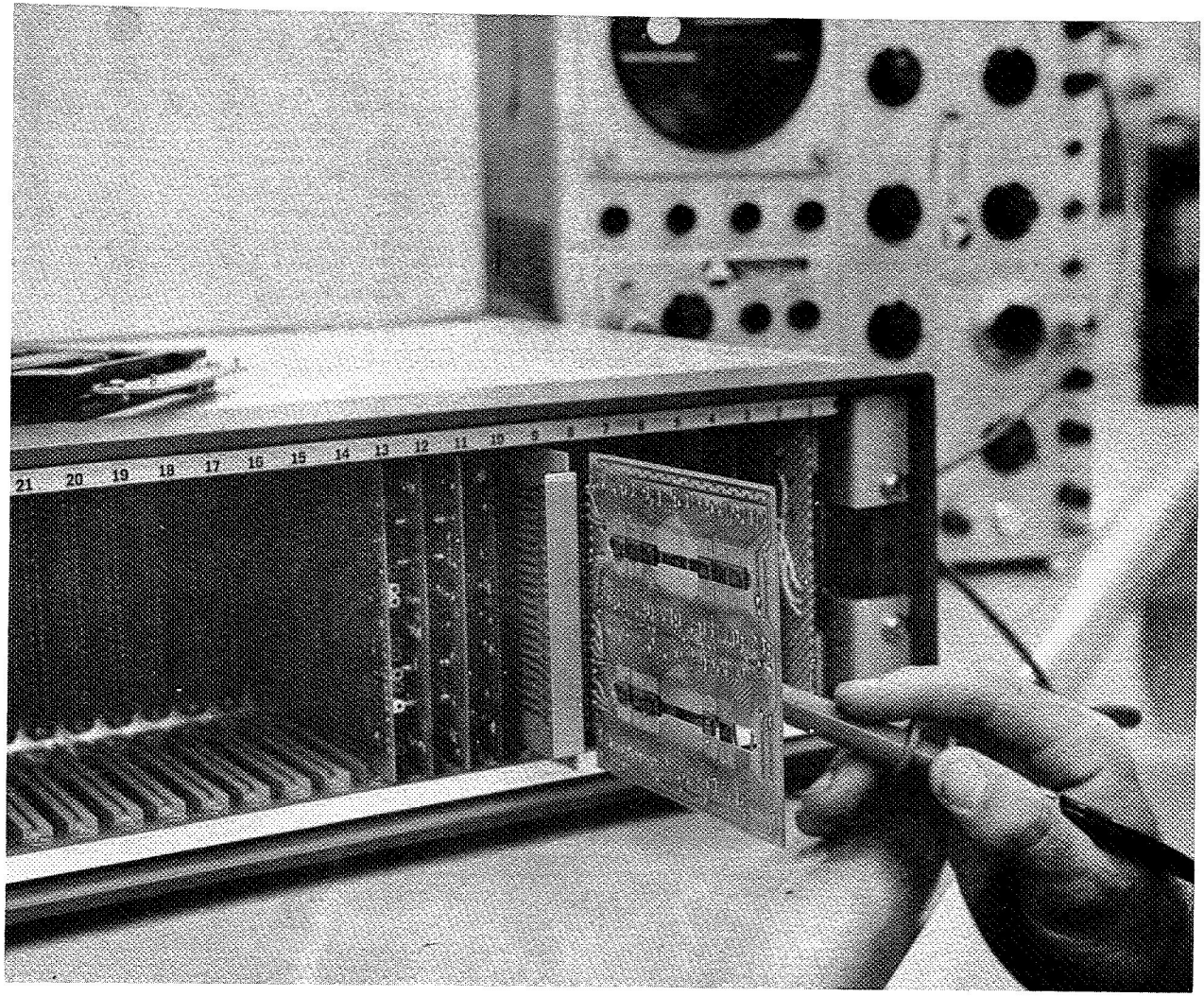


Figure C-2. Photograph of Breadboard Under Test

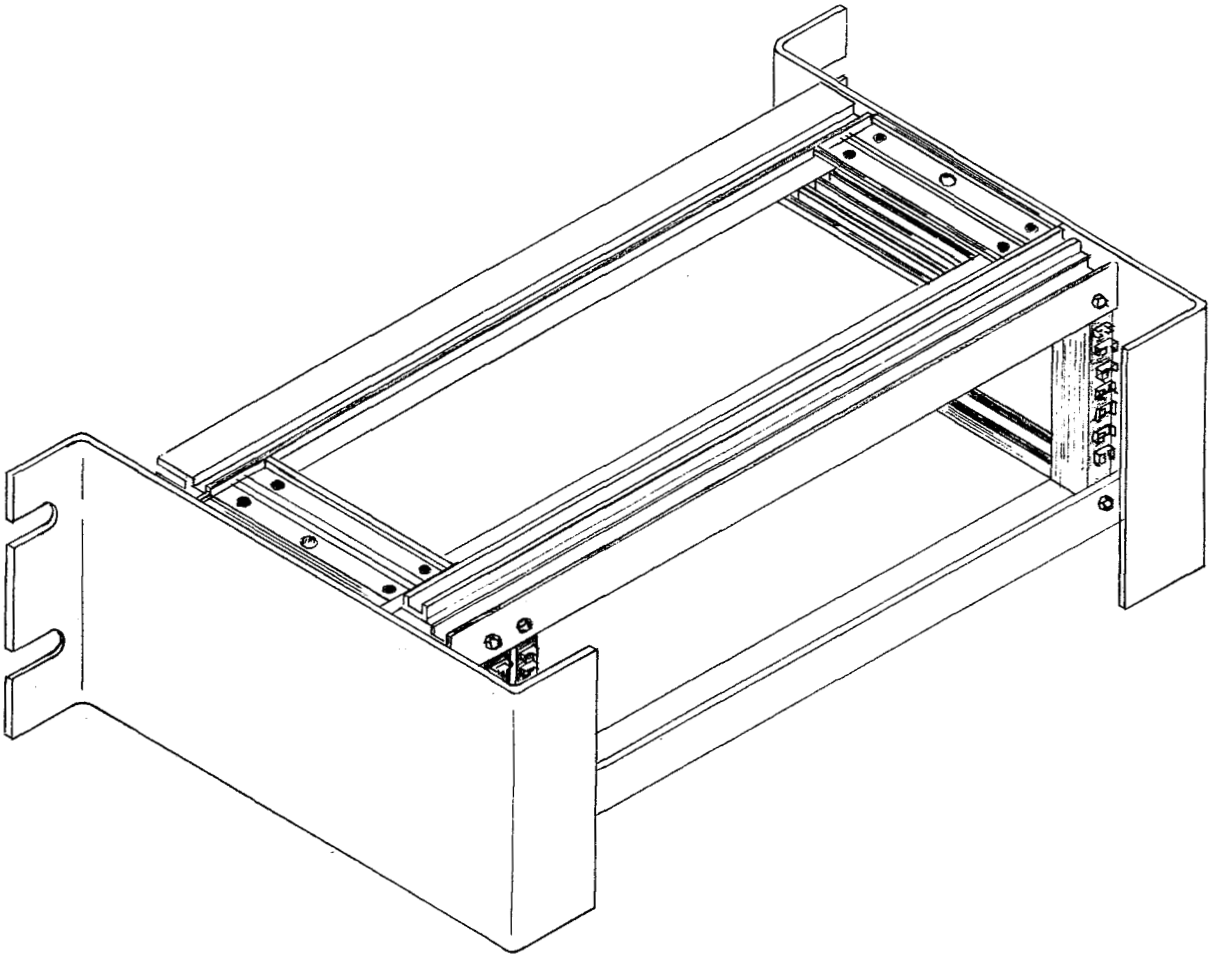


Figure C-3. Card File Assembly Drawing

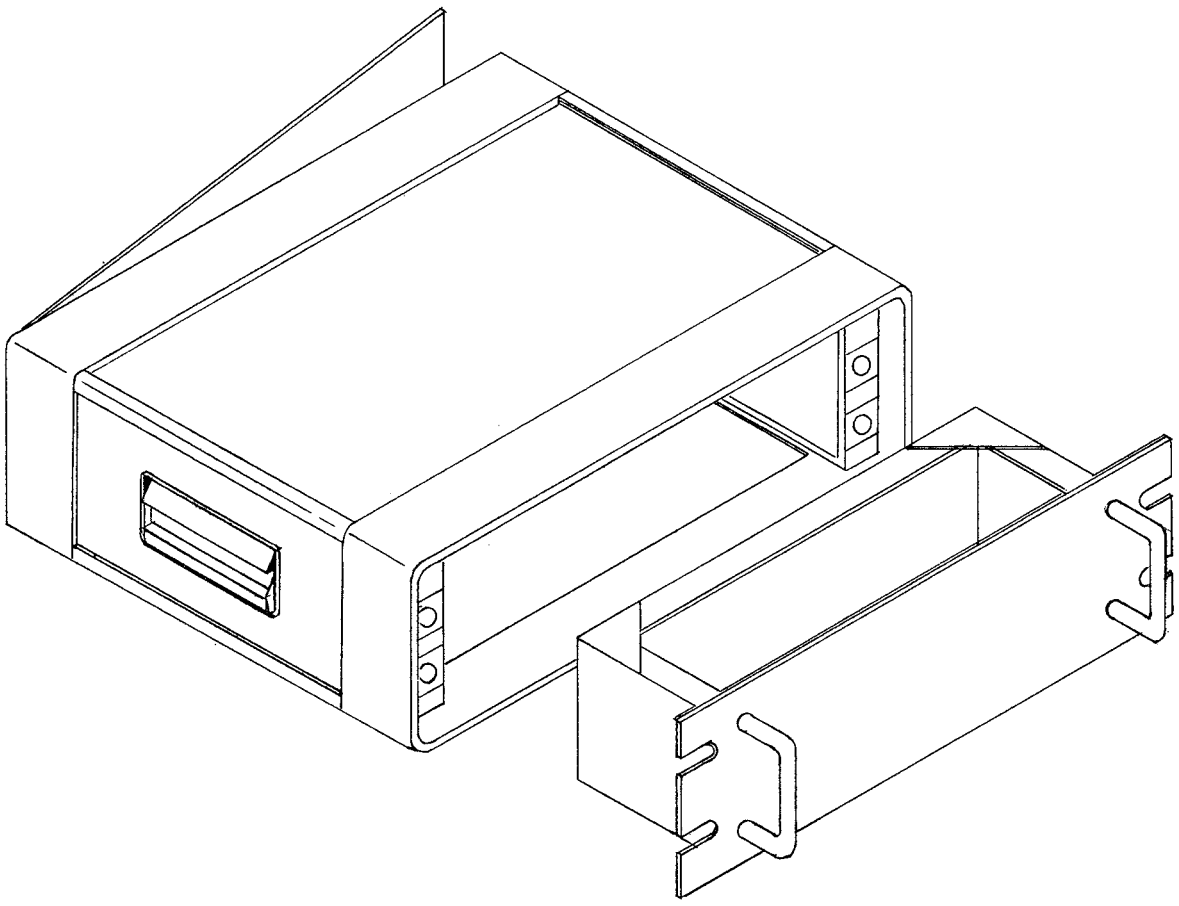
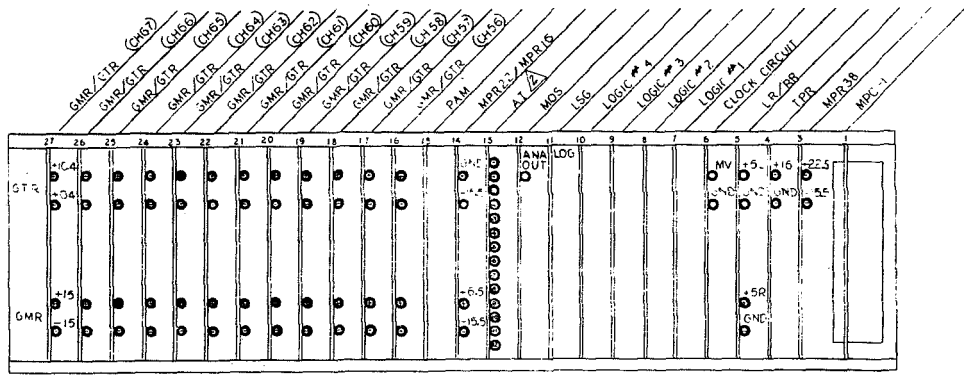


Figure C-4. Cabinet and Tester Assembly Drawing



LEGEND

MPC	= DC TO DC CONVERTER
MPR22	= MODIFIER PREREGULATOR 22 VOLTS OUTPUT
MPR16	= MODIFIER PREREGULATOR 16 VOLTS OUTPUT
MPR38	= MODIFIER PREREGULATOR 38 VOLTS OUTPUT
LR	= LOGIC REGULATOR
RR	= REFRENCE REGULATOR
LSG	= LEVEL SHIFT GATES
MOS	= MOSFET MULTIPLEX SWITCHES
PAM	= PAM OUTPUT CIRCUIT
AI	= ANALOG INPUT
GMR	= GATED MODIFIER REGULATOR
GTR	= GATED TRANSDUCER REGULATOR

Fig. C-5. Card File - Card Positions

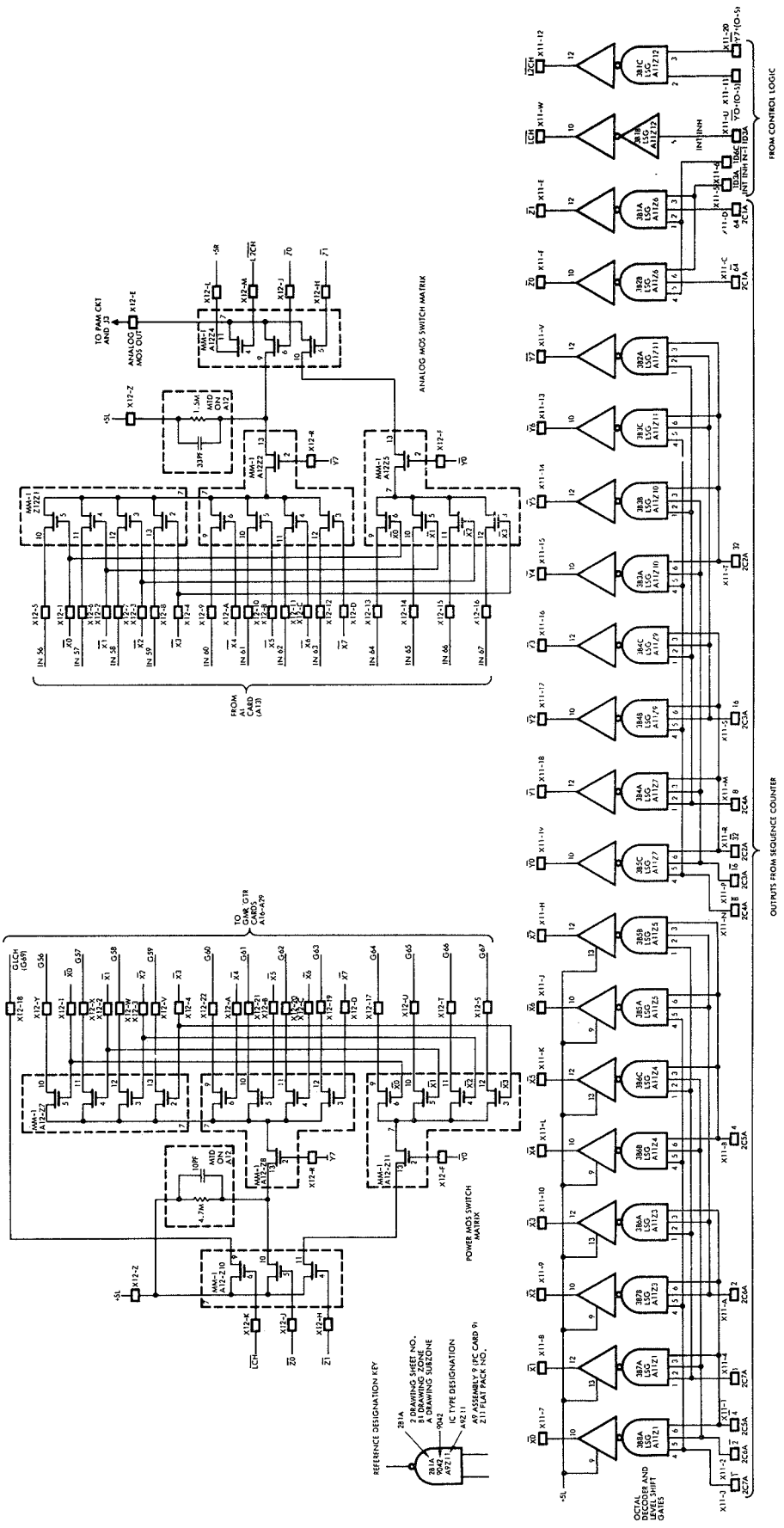


Figure C-6. Logic Diagram - Switches and Drivers

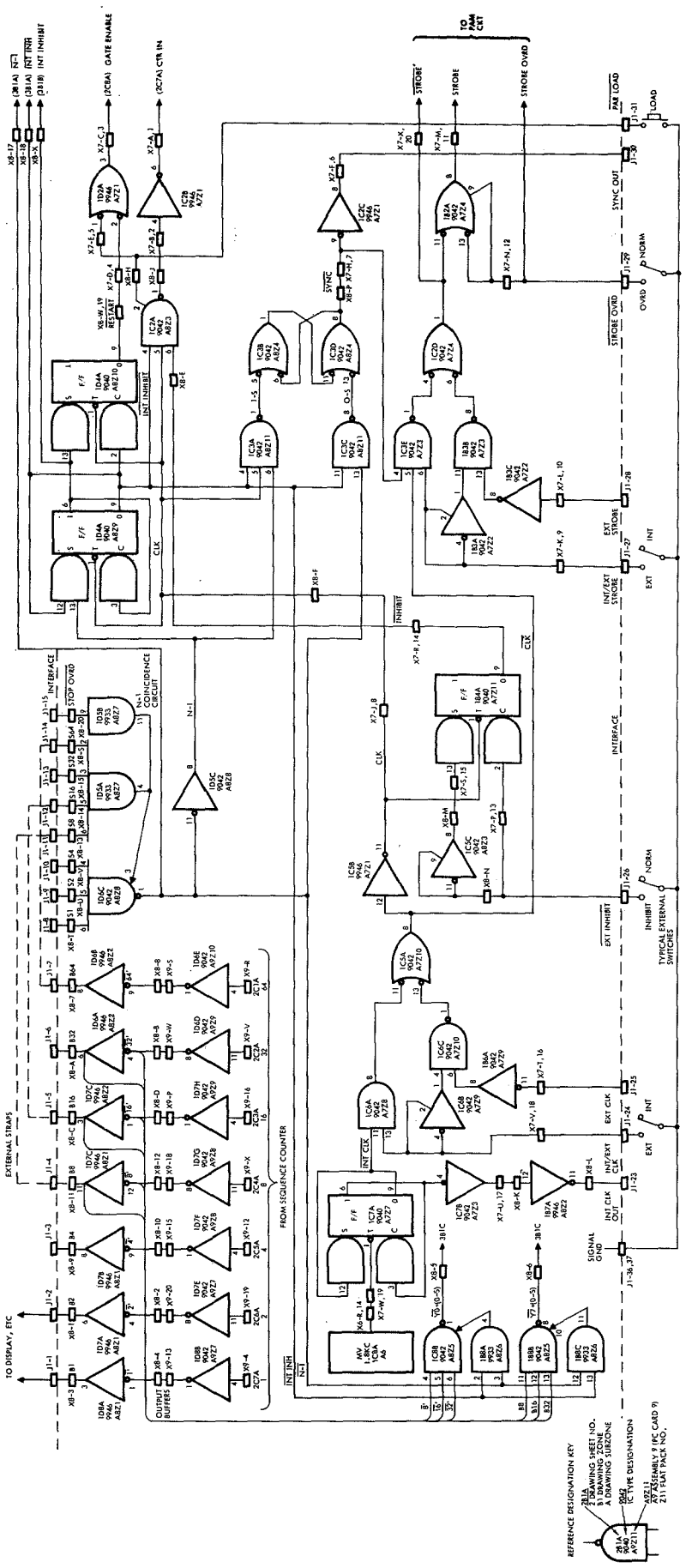


Fig. C-7. Logic Diagram - Control

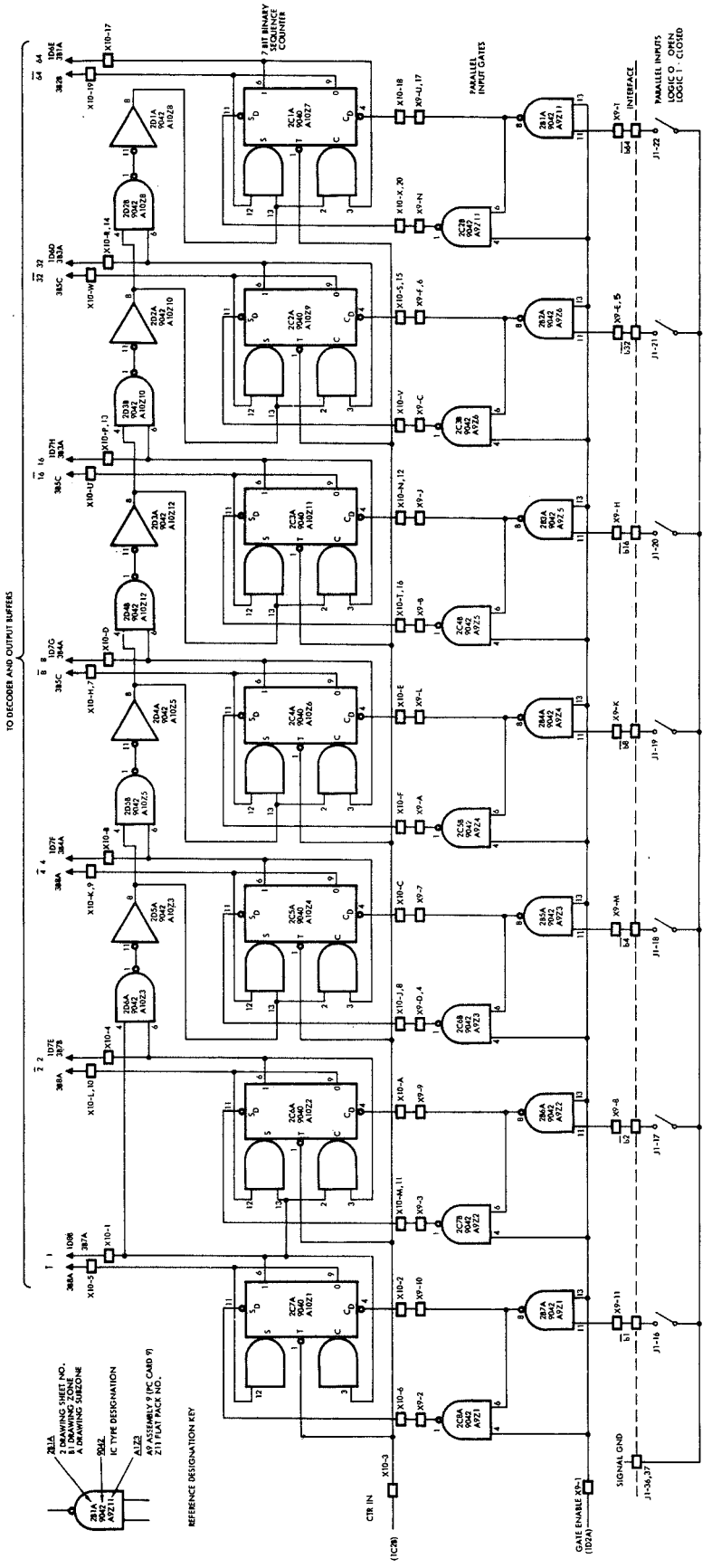


Fig. C-8. Logic Diagram - Counter

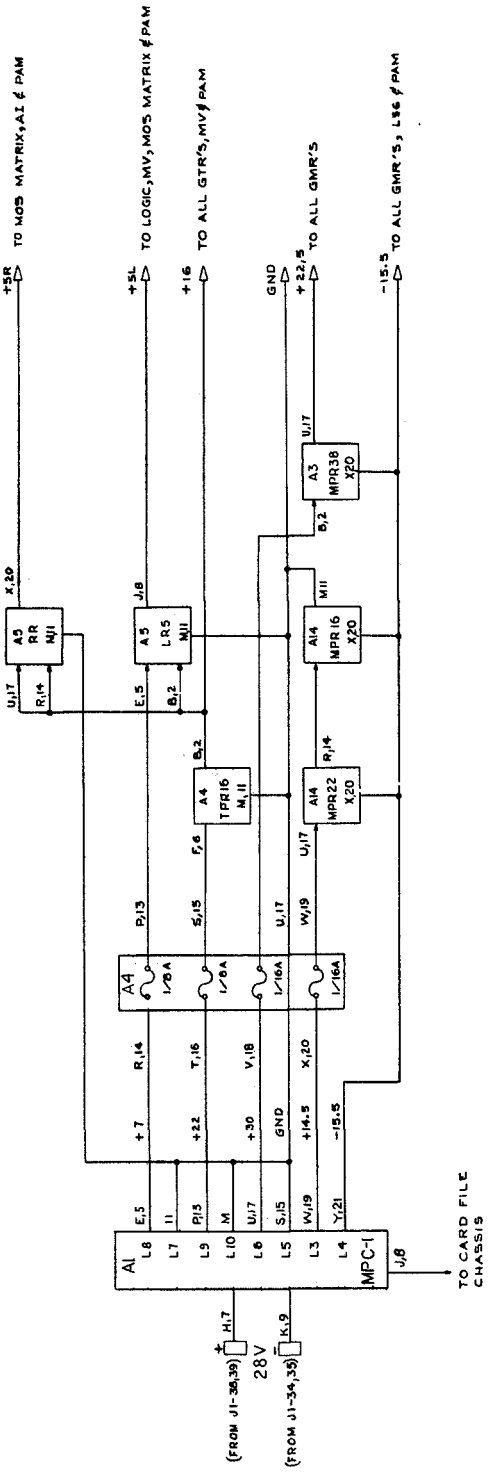


Fig. C-9. Power Distribution

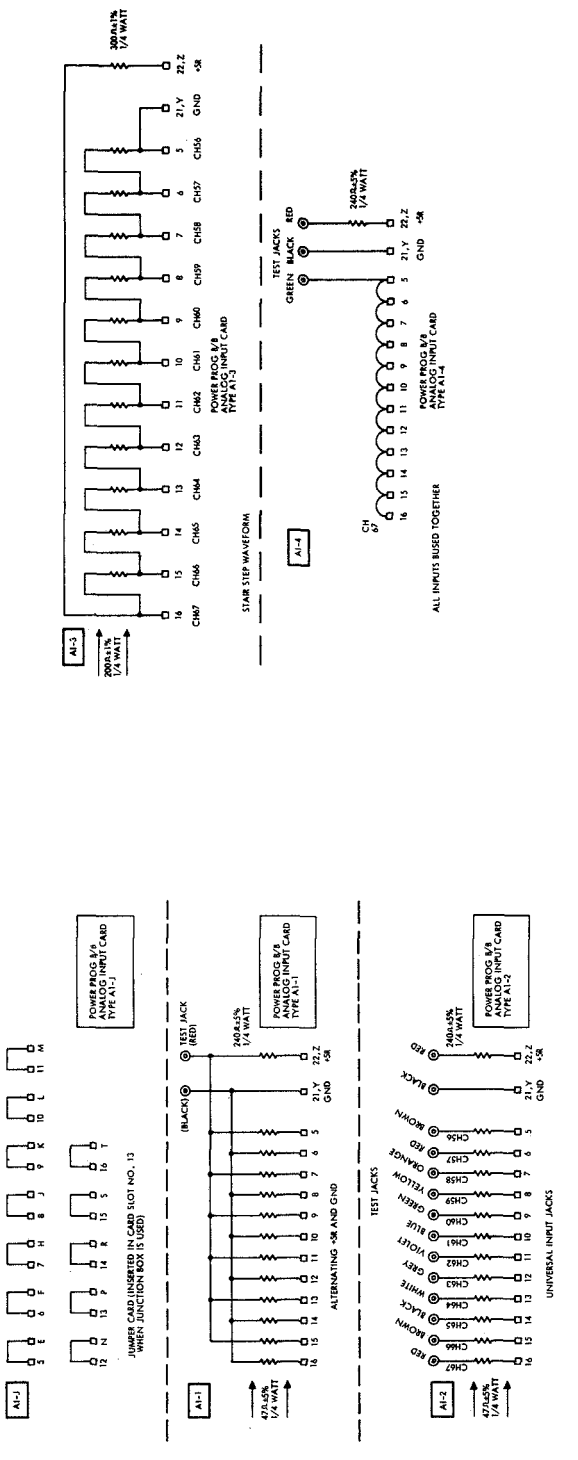


Fig. C-10. Analog Input Options

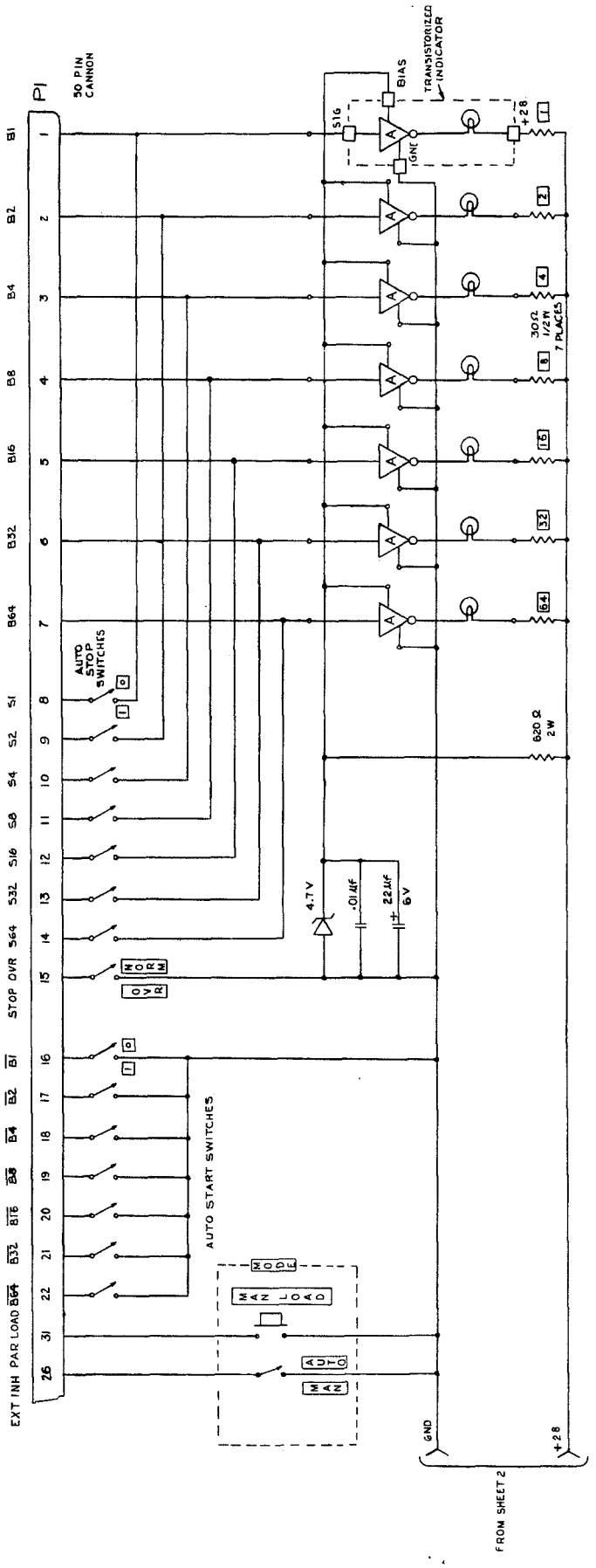


Fig. C-11. Test Unit Indicators

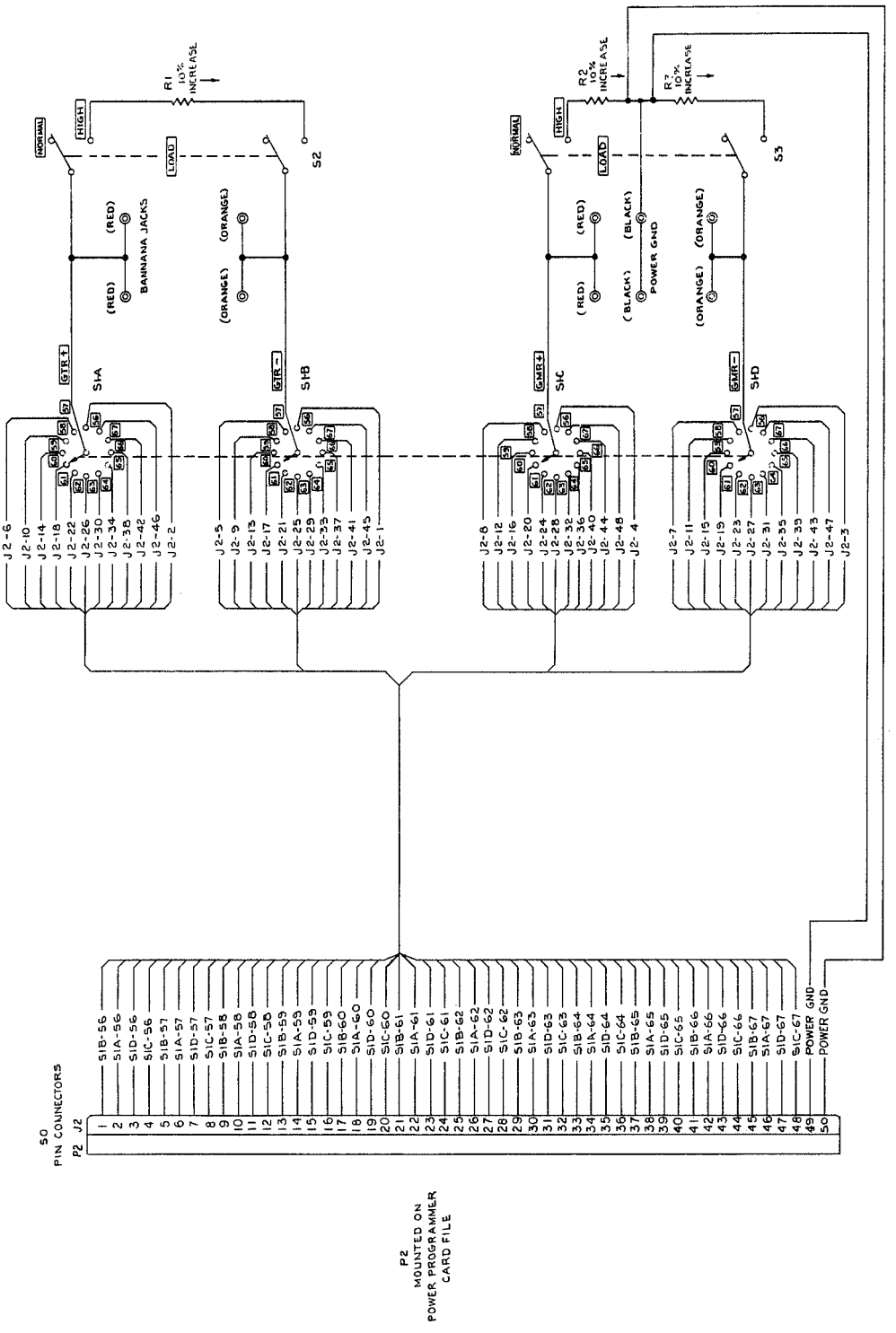


Fig. C-12. Junction Box Switches

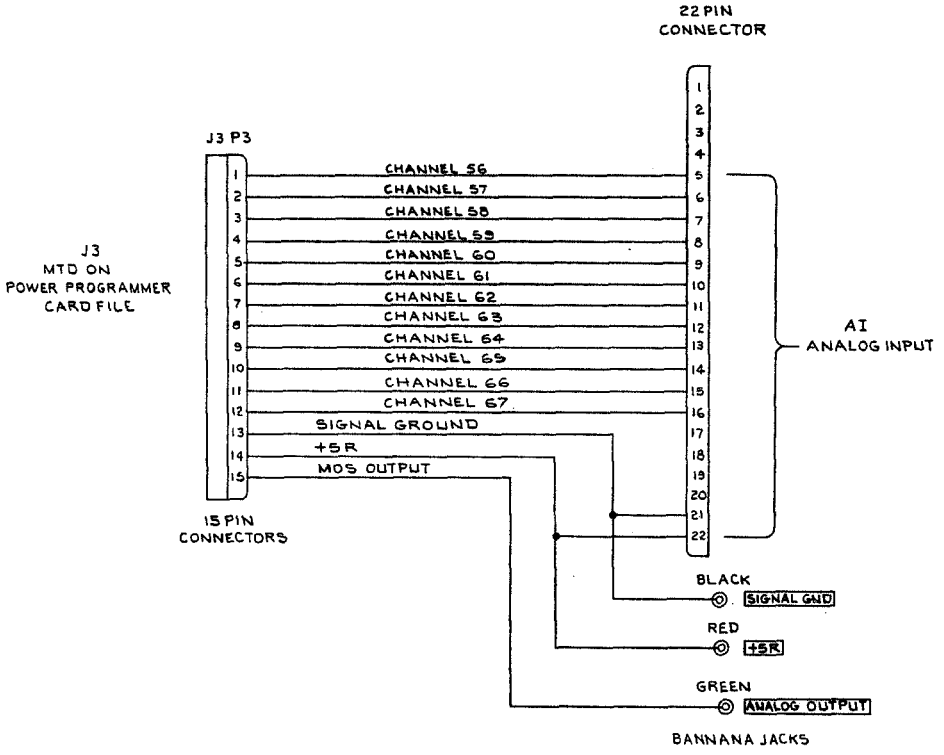


Fig. C-13. Junction Box Connector

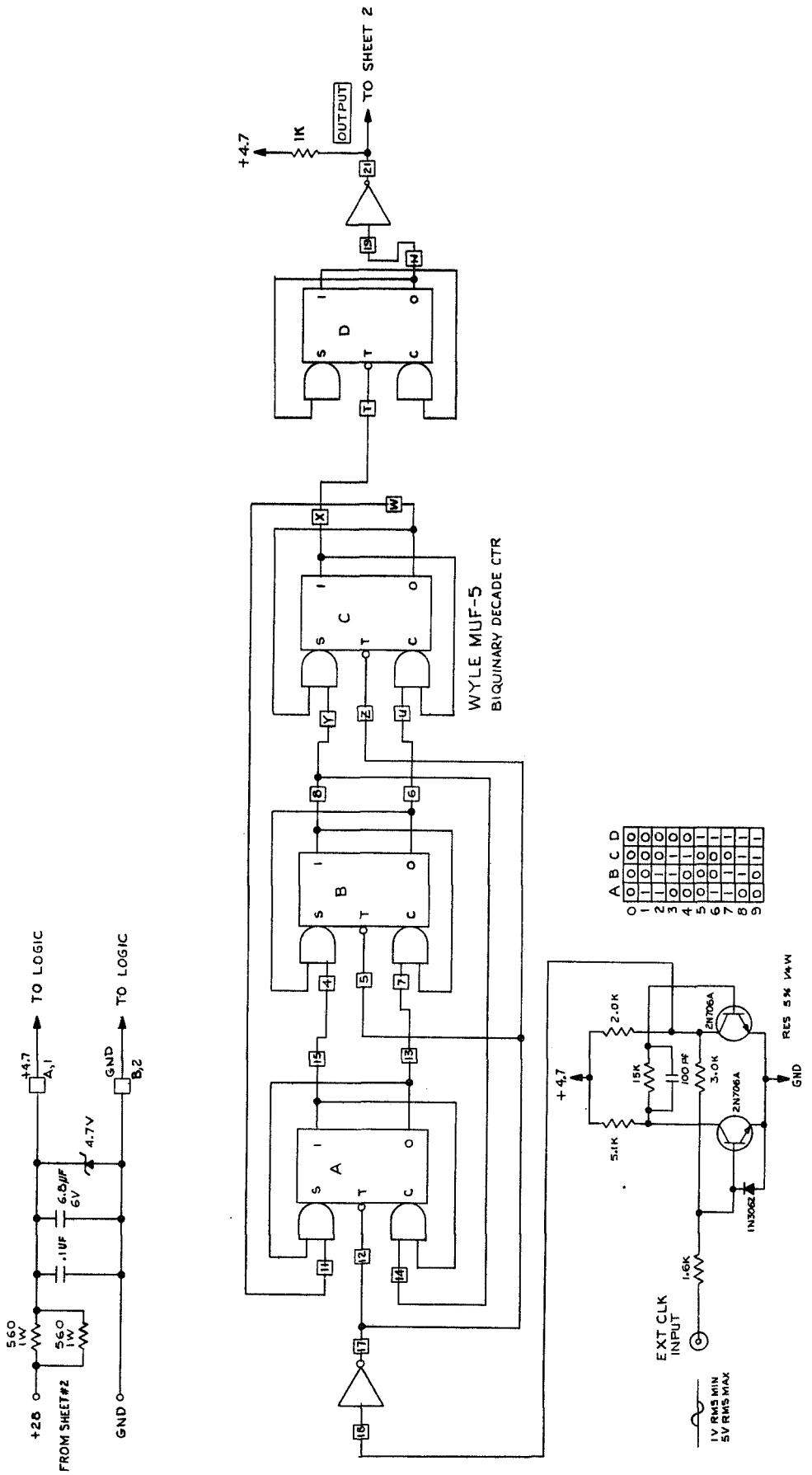


Fig. C-14. Test Unit Frequency Divider

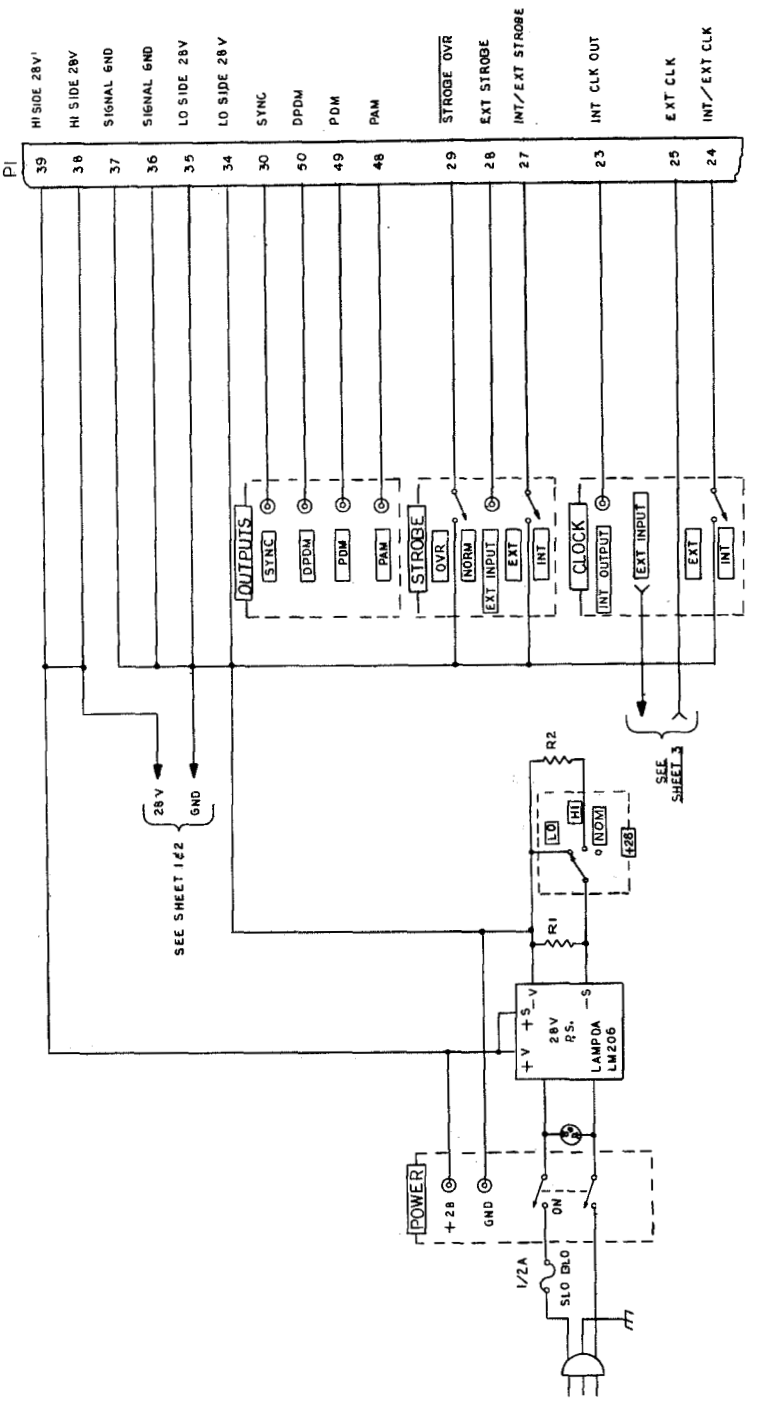


Fig. C-15. Test Unit Connector

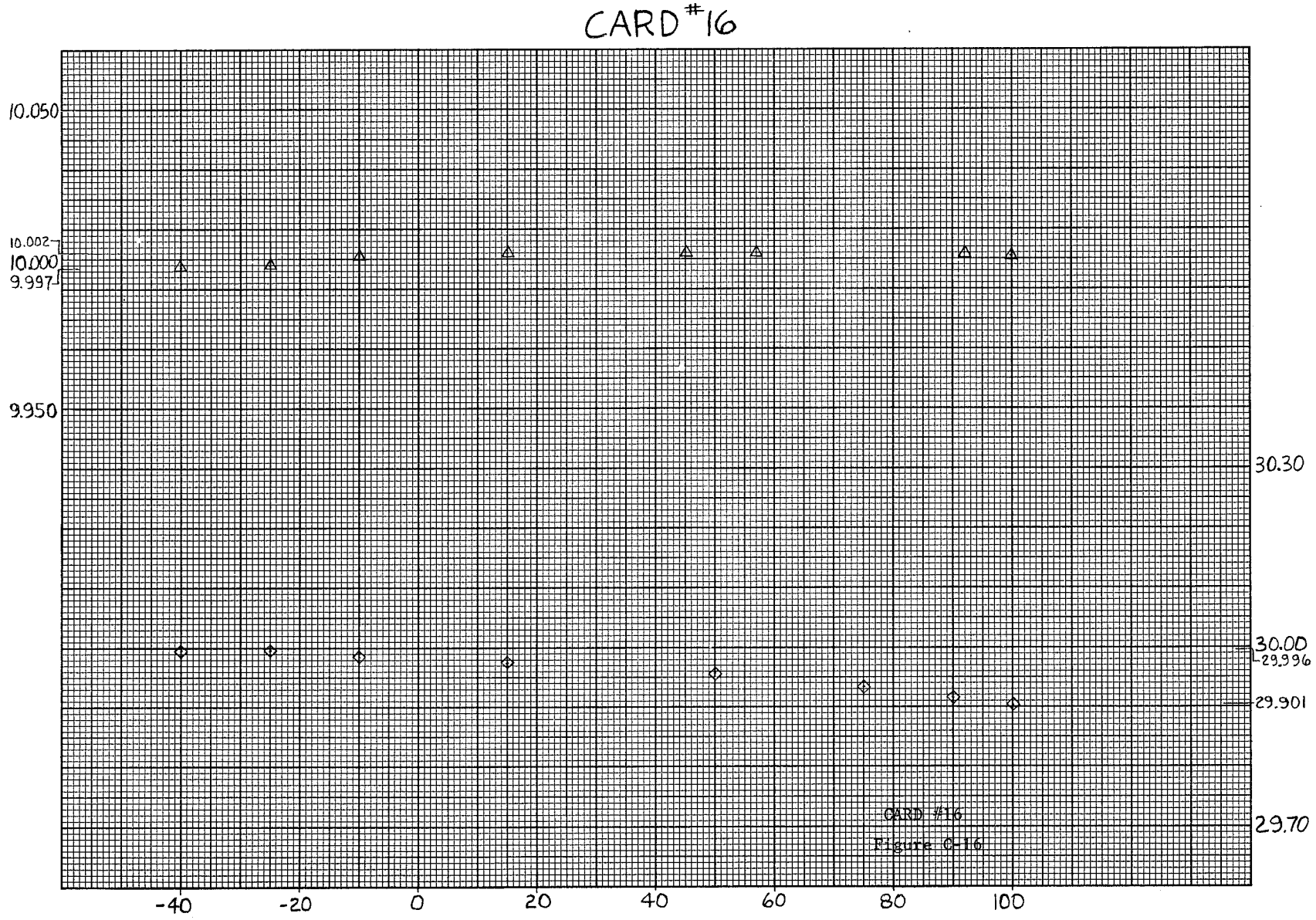


Figure C-16. Regulator Voltages vs. Temperature Card No. 16

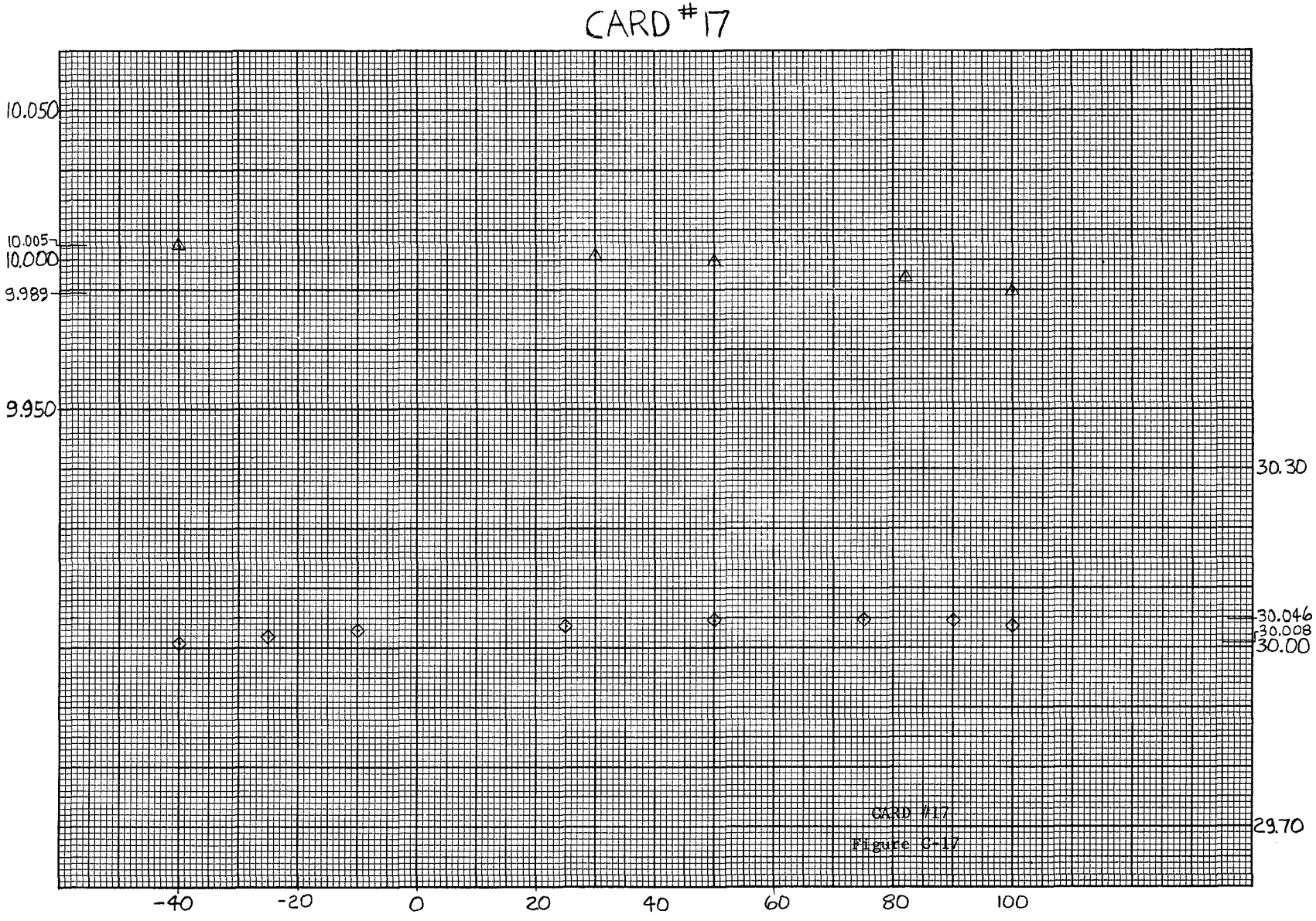


Figure C-17. Regulator Voltages vs. Temperature Card No. 17

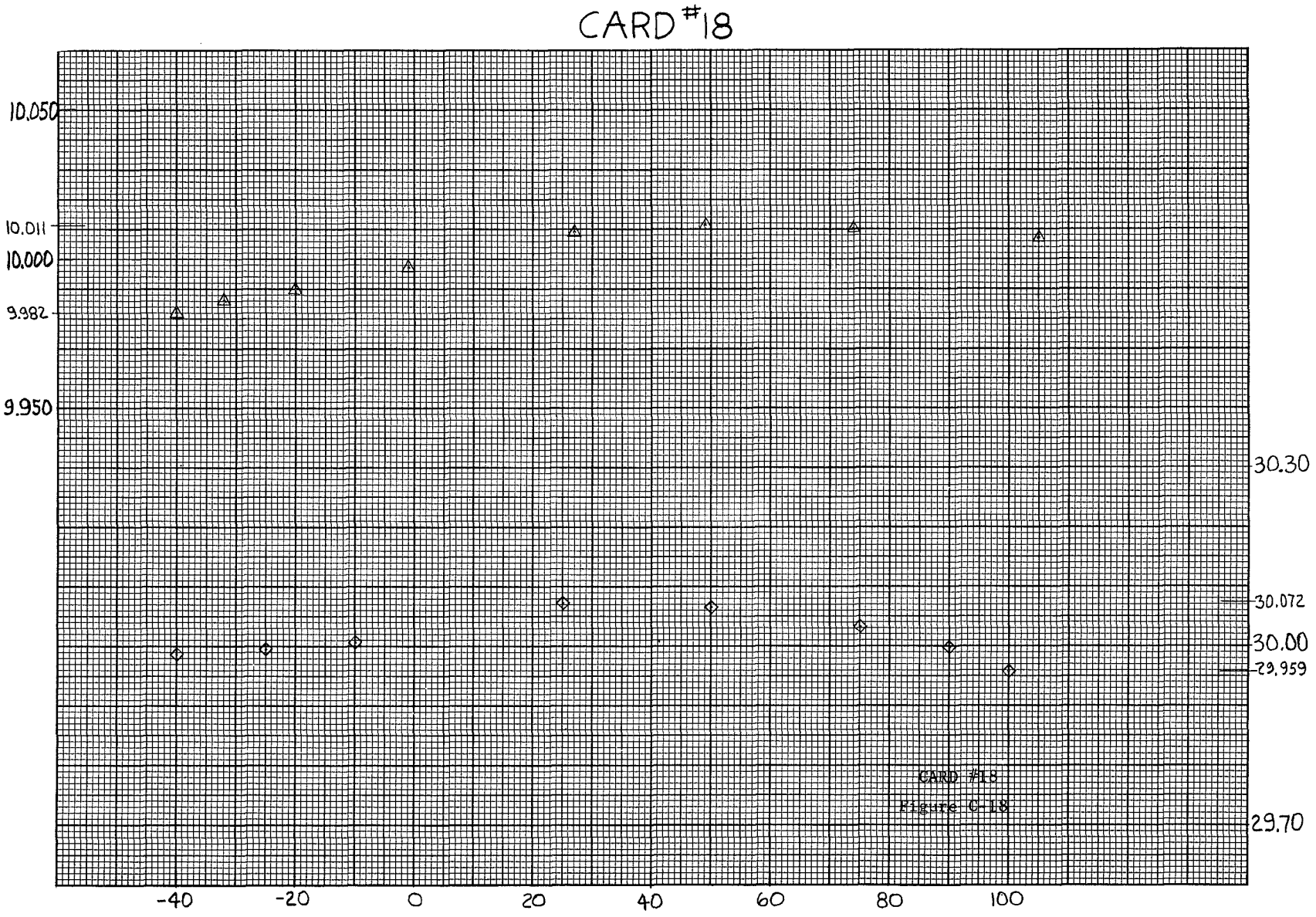


Figure C-18. Regulator Voltages vs. Temperature Card No. 18

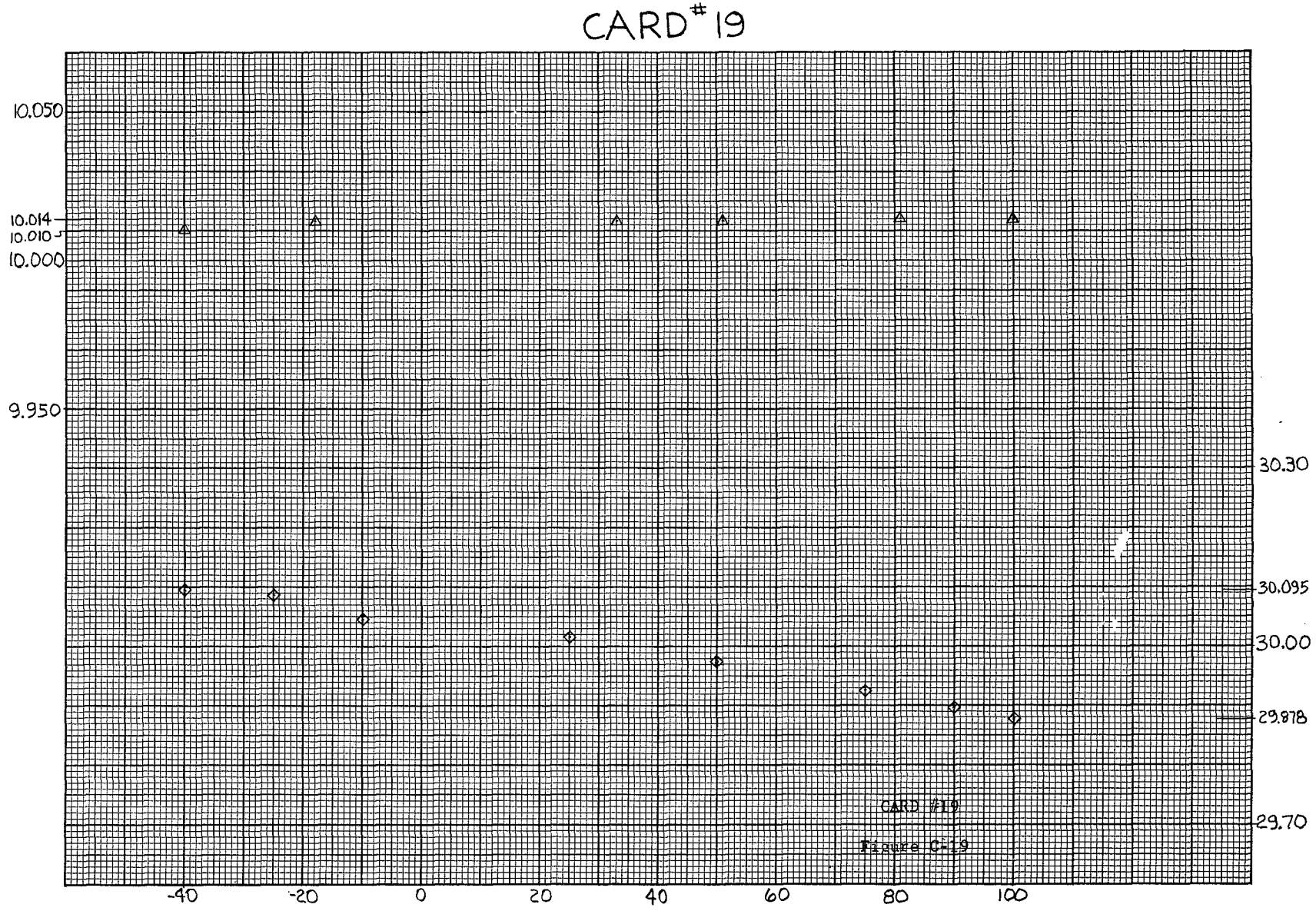


Figure C-19. Regulator Voltages vs. Temperature Card No. 19

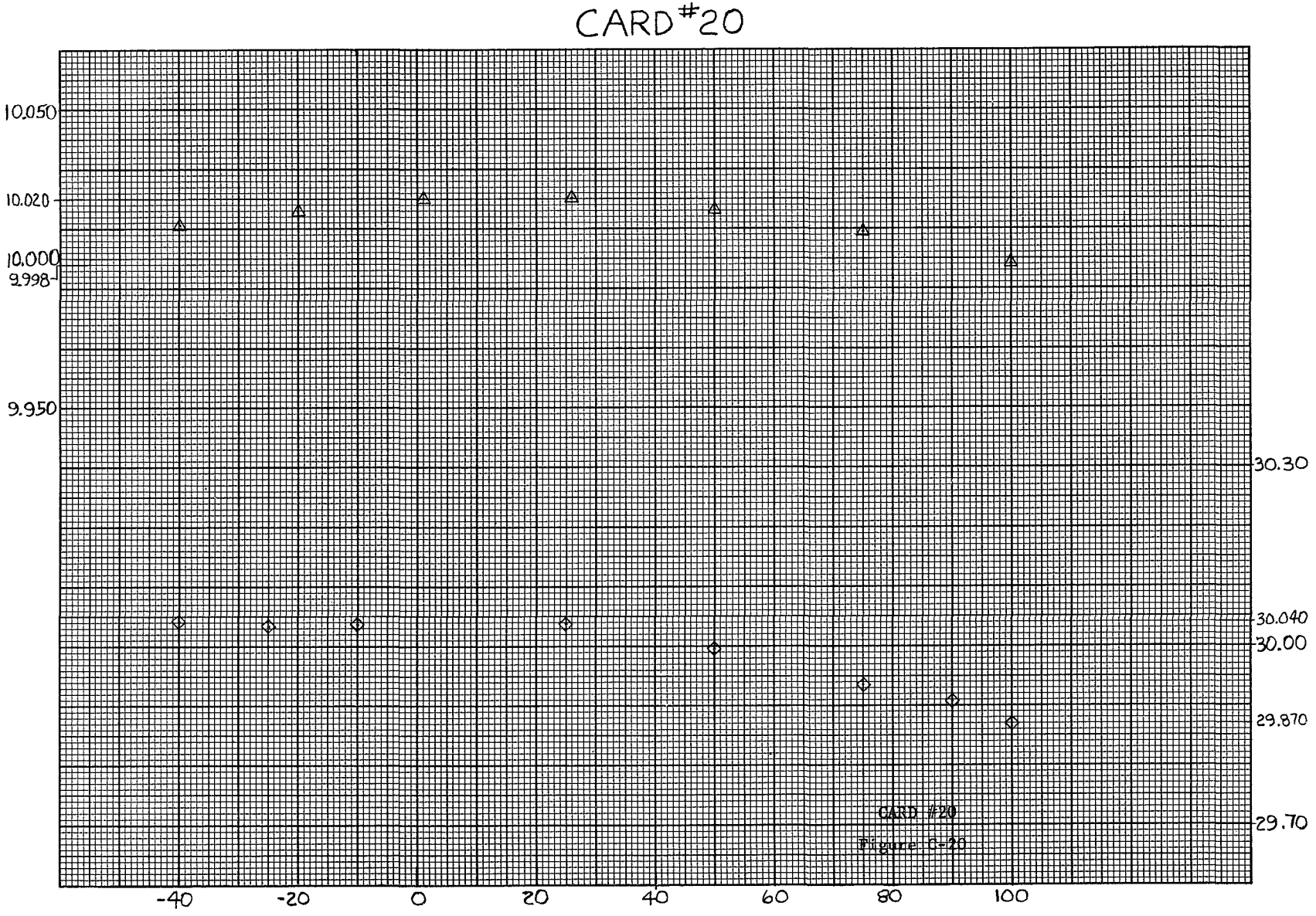


Figure C-20. Regulator Voltages vs. Temperature Card No. 20

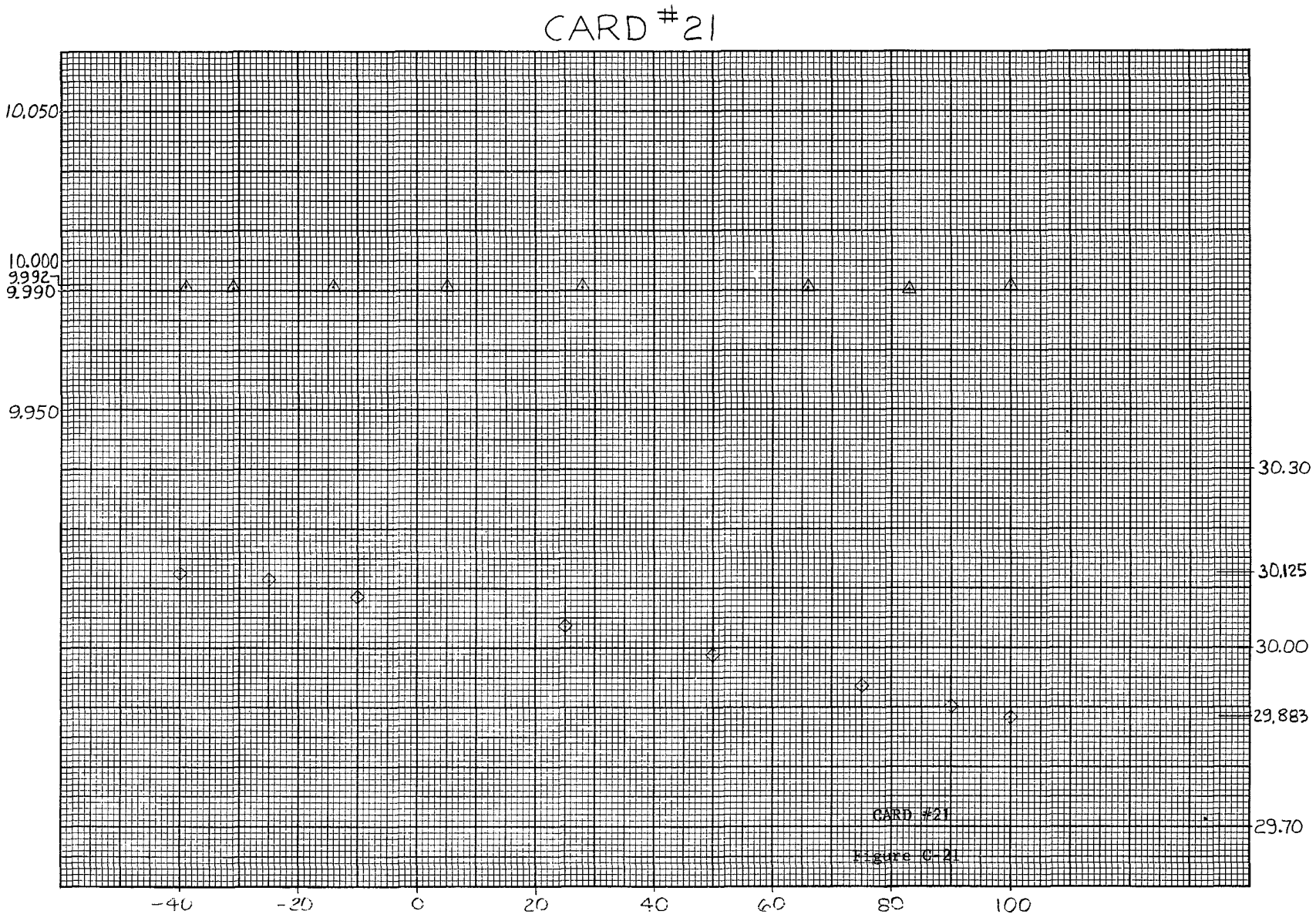


Figure C-21. Regulator Voltages vs. Temperature Card No. 21

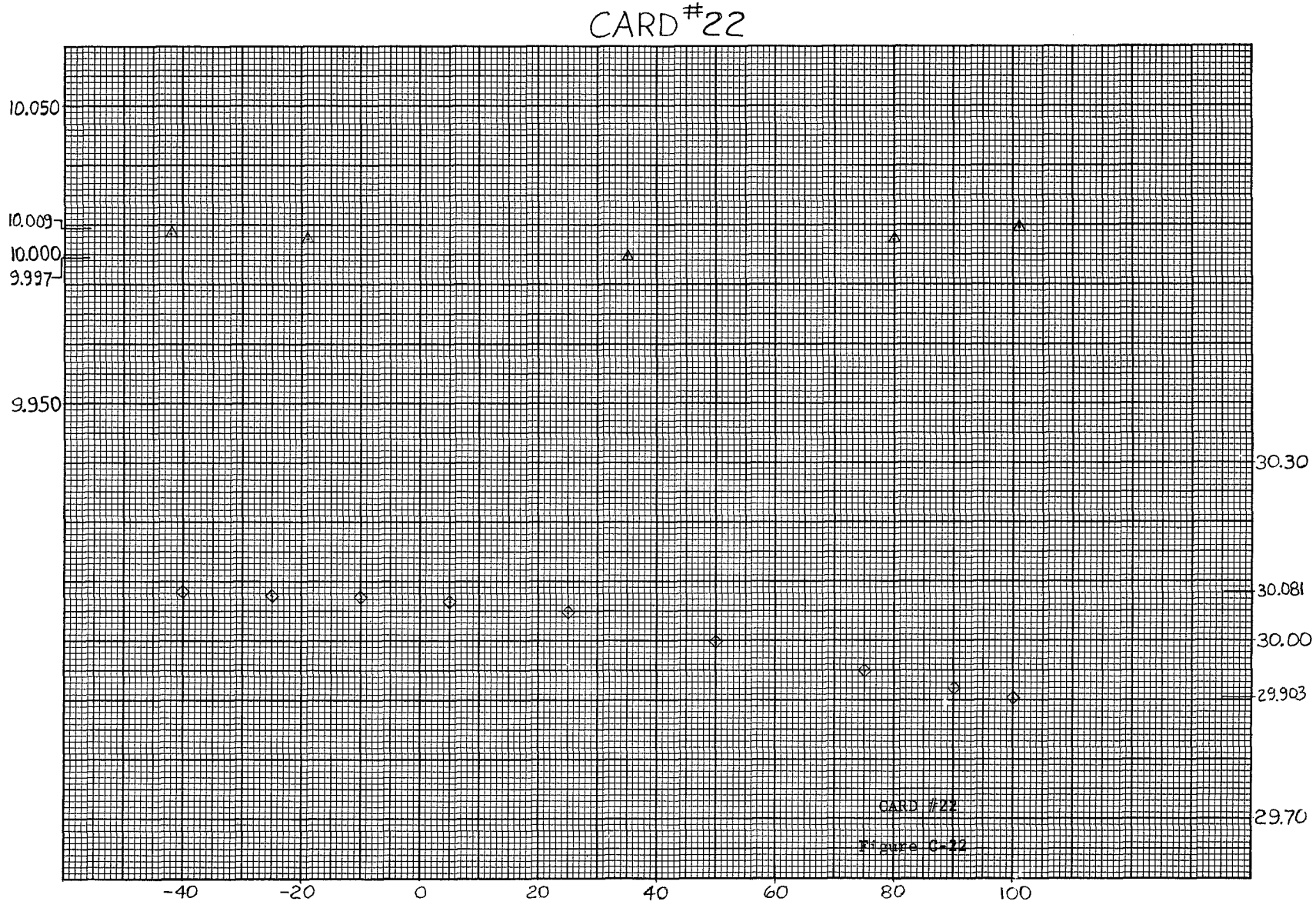


Figure C-22. Regulator Voltages vs. Temperature Card No. 22

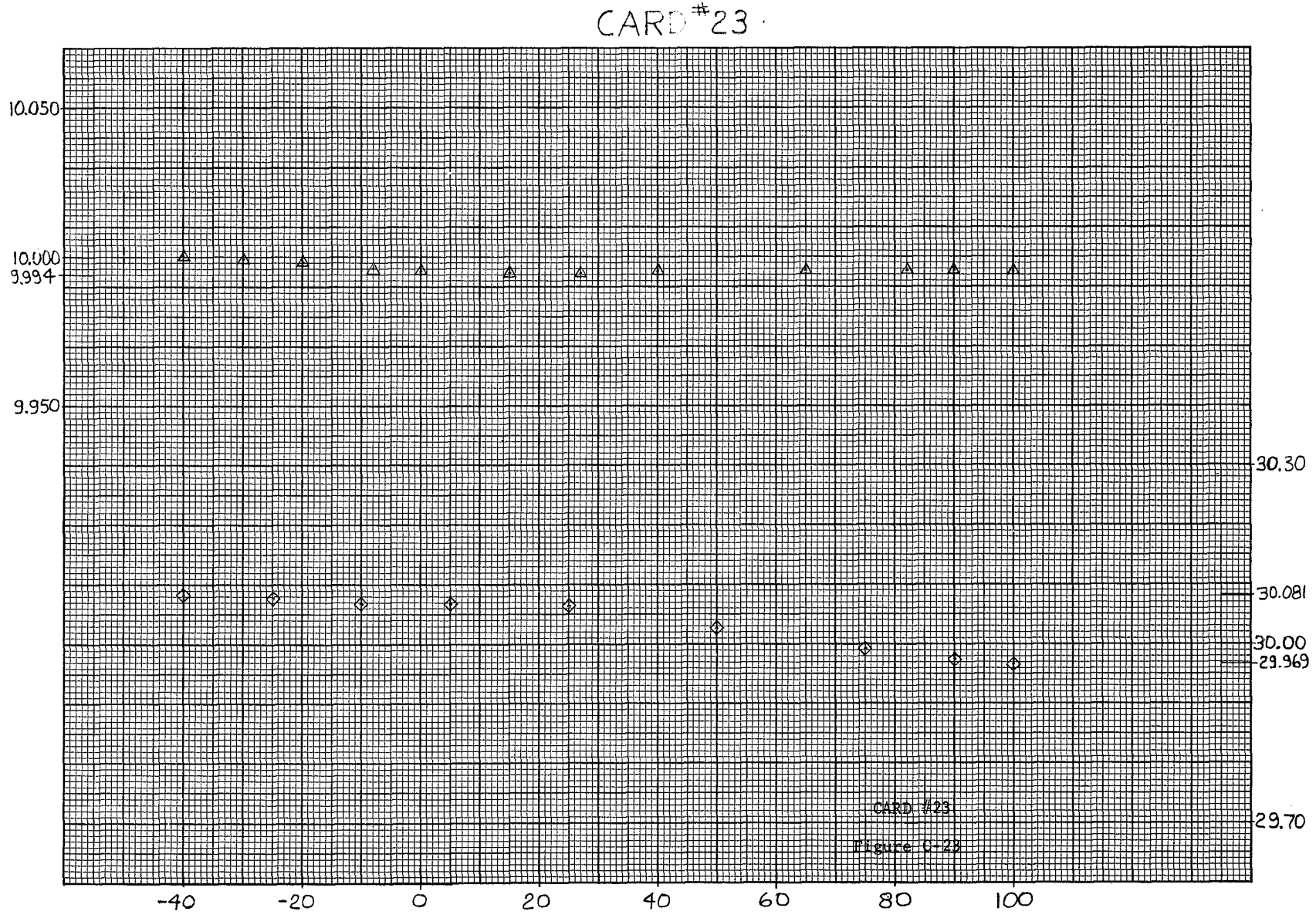


Figure C-23. Regulator Voltages vs. Temperature Card No. 23

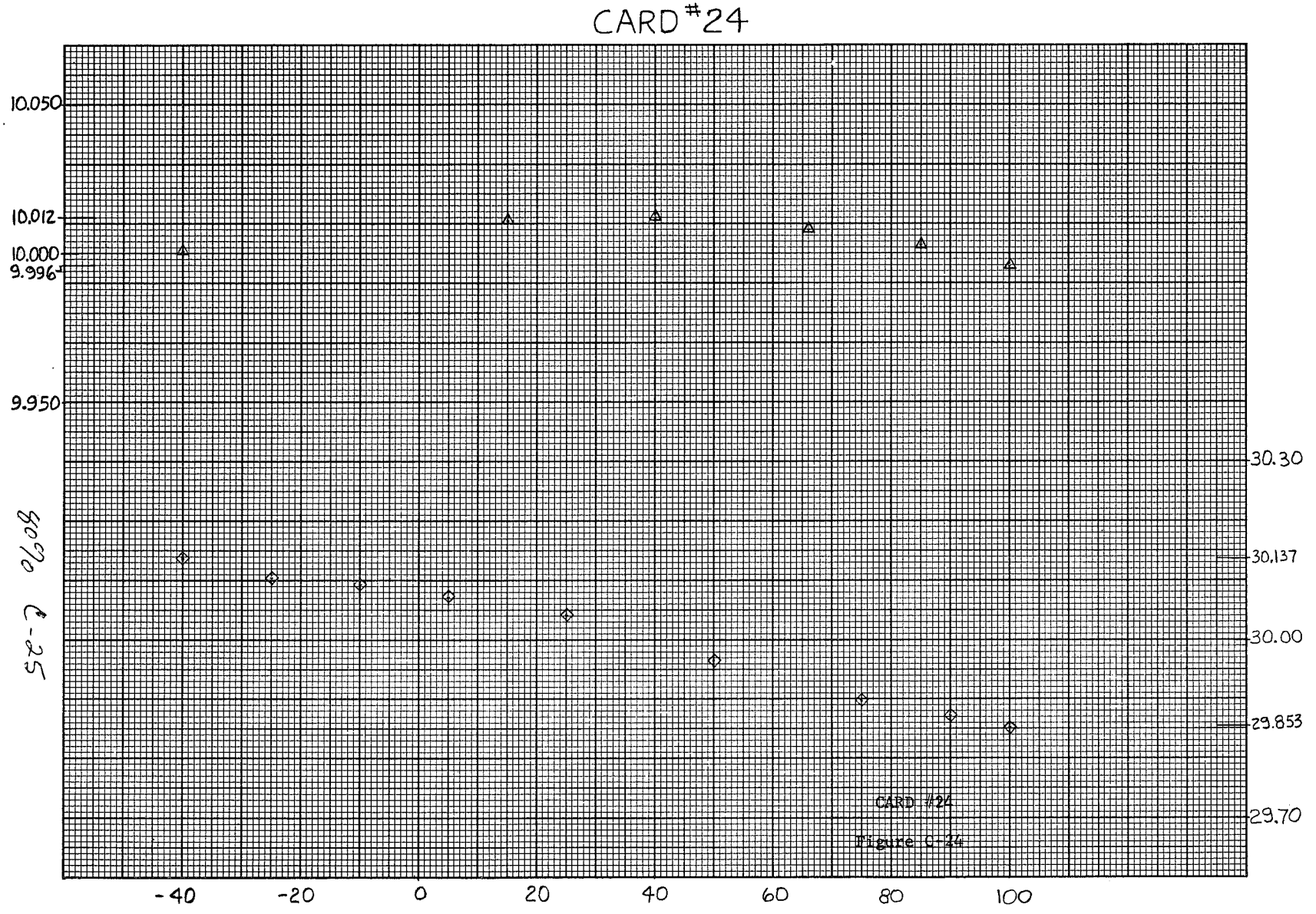


Figure C-24. Regulator Voltages vs. Temperature Card No. 24

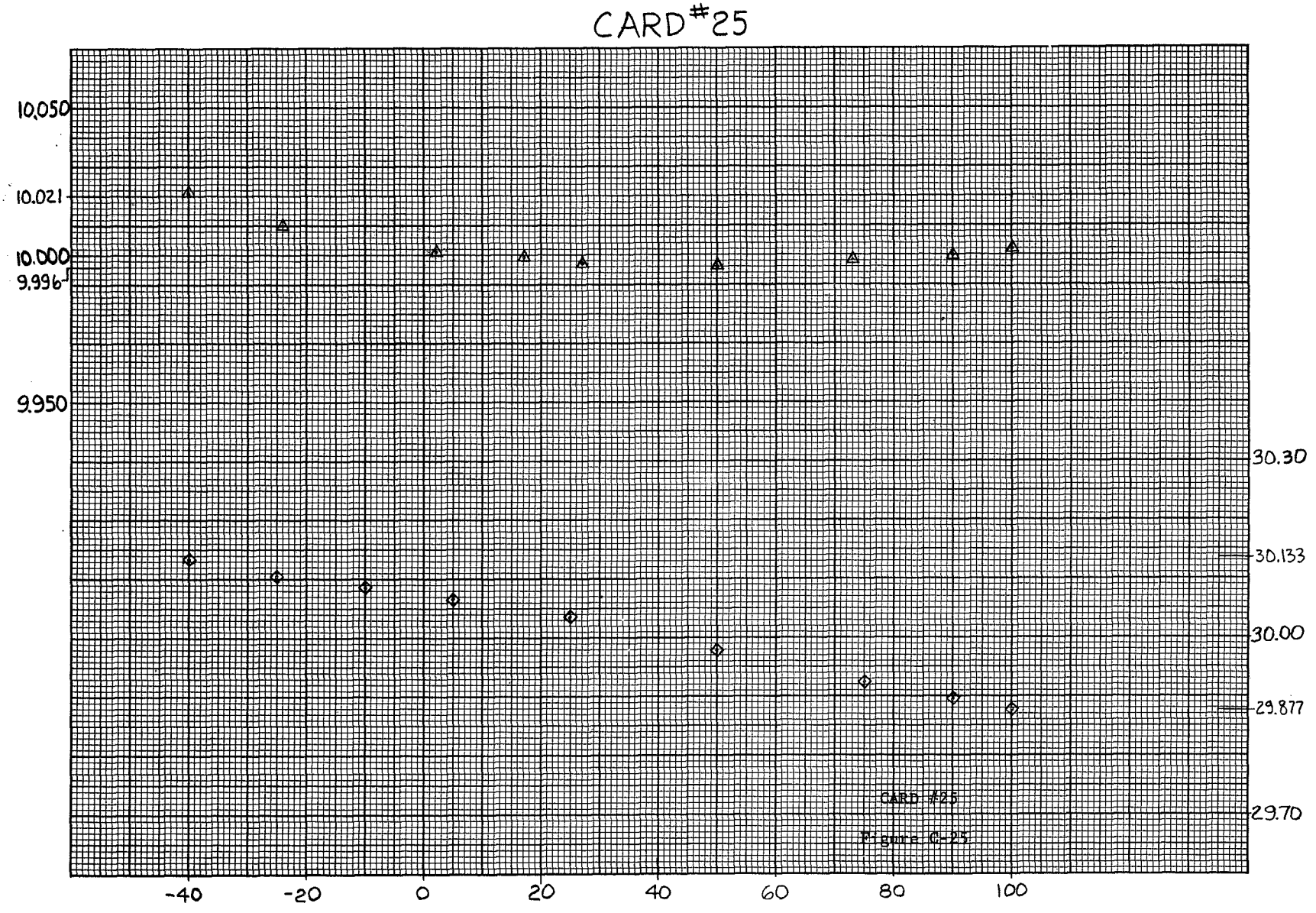


Figure C-25. Regulator Voltages vs. Temperature Card No. 25

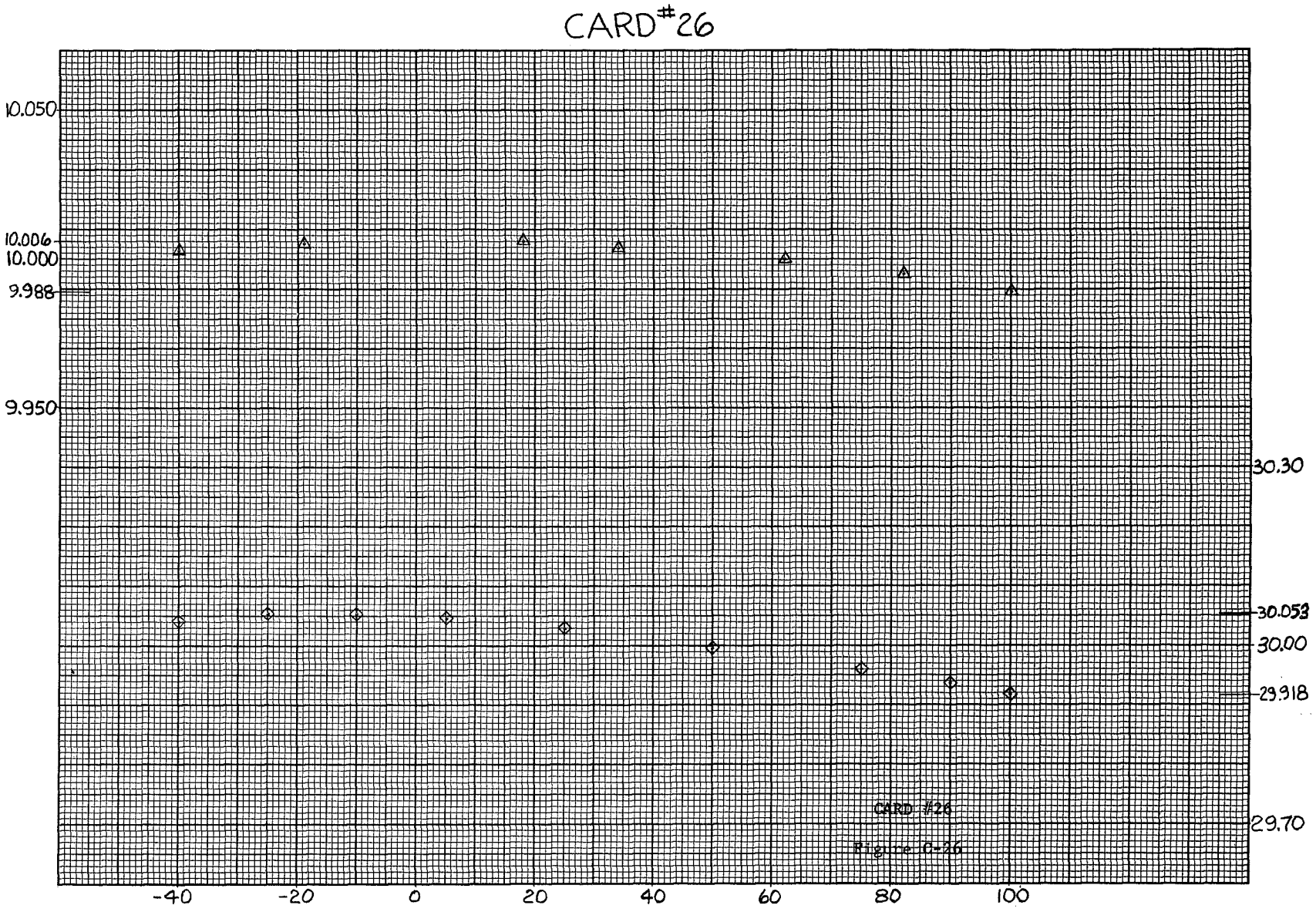


Figure C-26. Regulator Voltages vs. Temperature Card No. 26

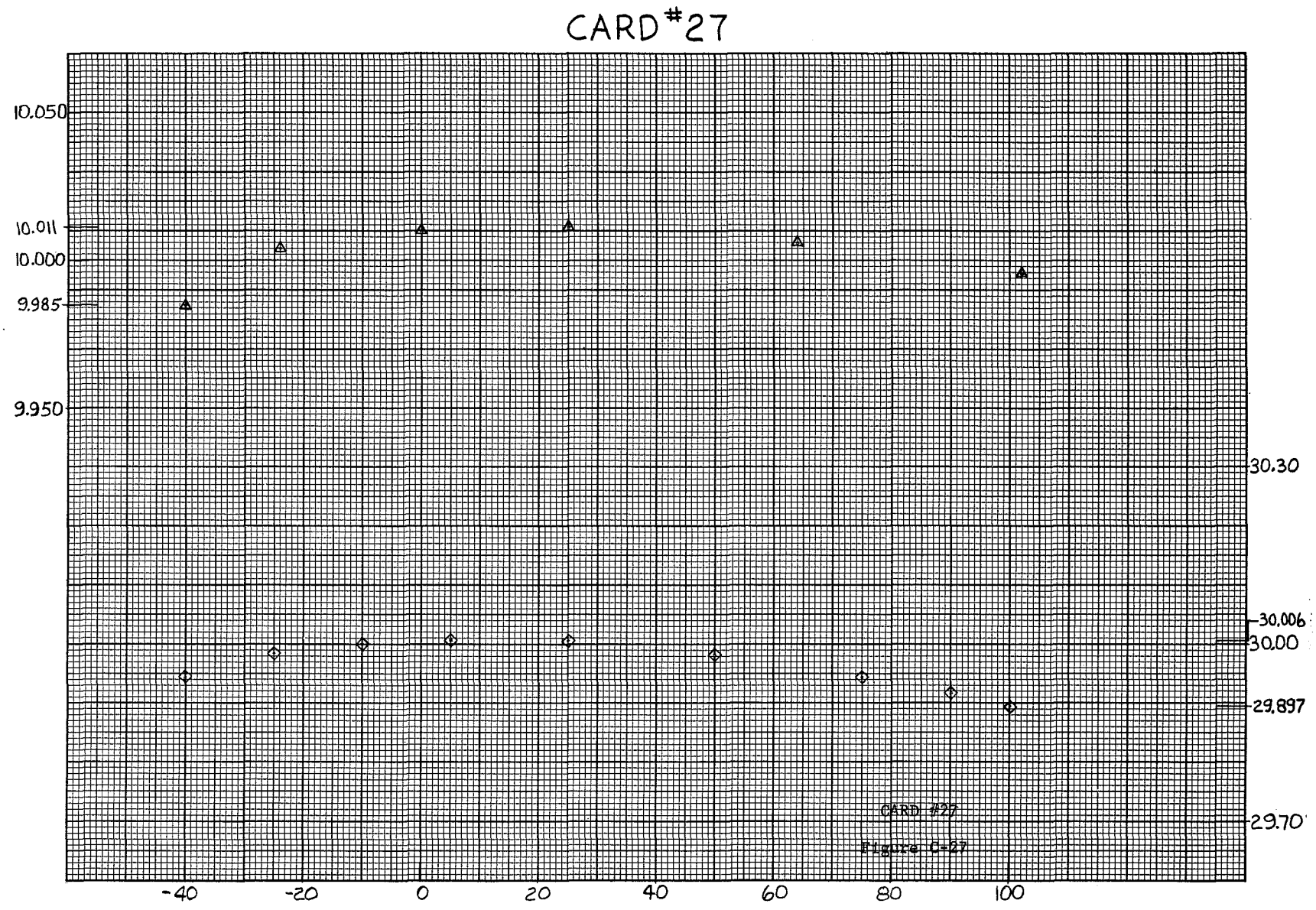


Figure C-27. Regulator Voltages vs. Temperature Card No. 27

APPENDIX D

POWER CONVERTER THERMAL ANALYSIS

APPENDIX D

POWER CONVERTER THERMAL ANALYSIS

A thermal analysis was performed on the power converter package.

Figures D-1 and D-2 show the heat dissipation calculations for the overall power converter package and the integrated circuit flat package. The analysis which follows is based on the information on the two figures. The results are summarized at the end.

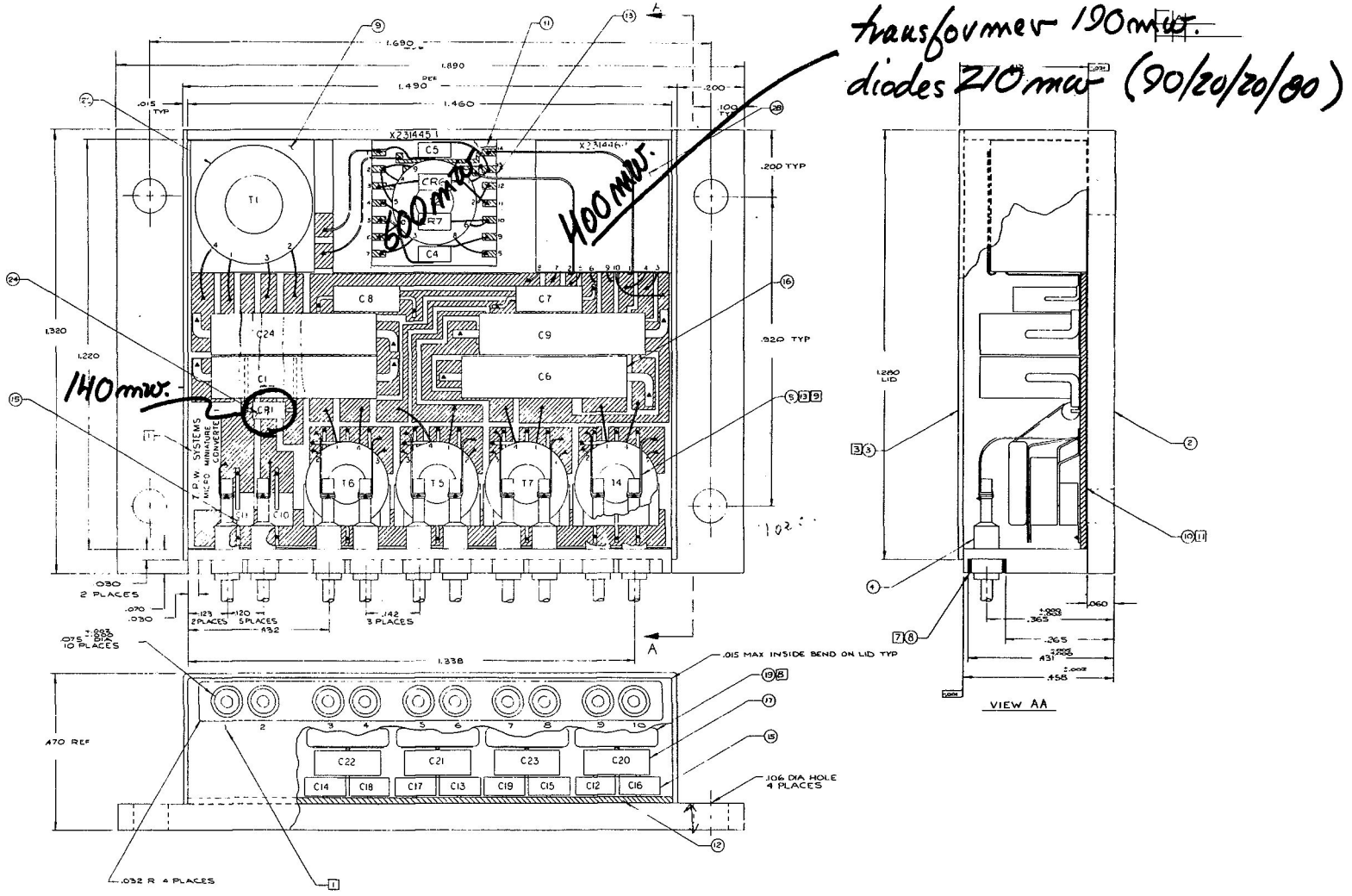


Figure D-1. Overall Package Heat Levels

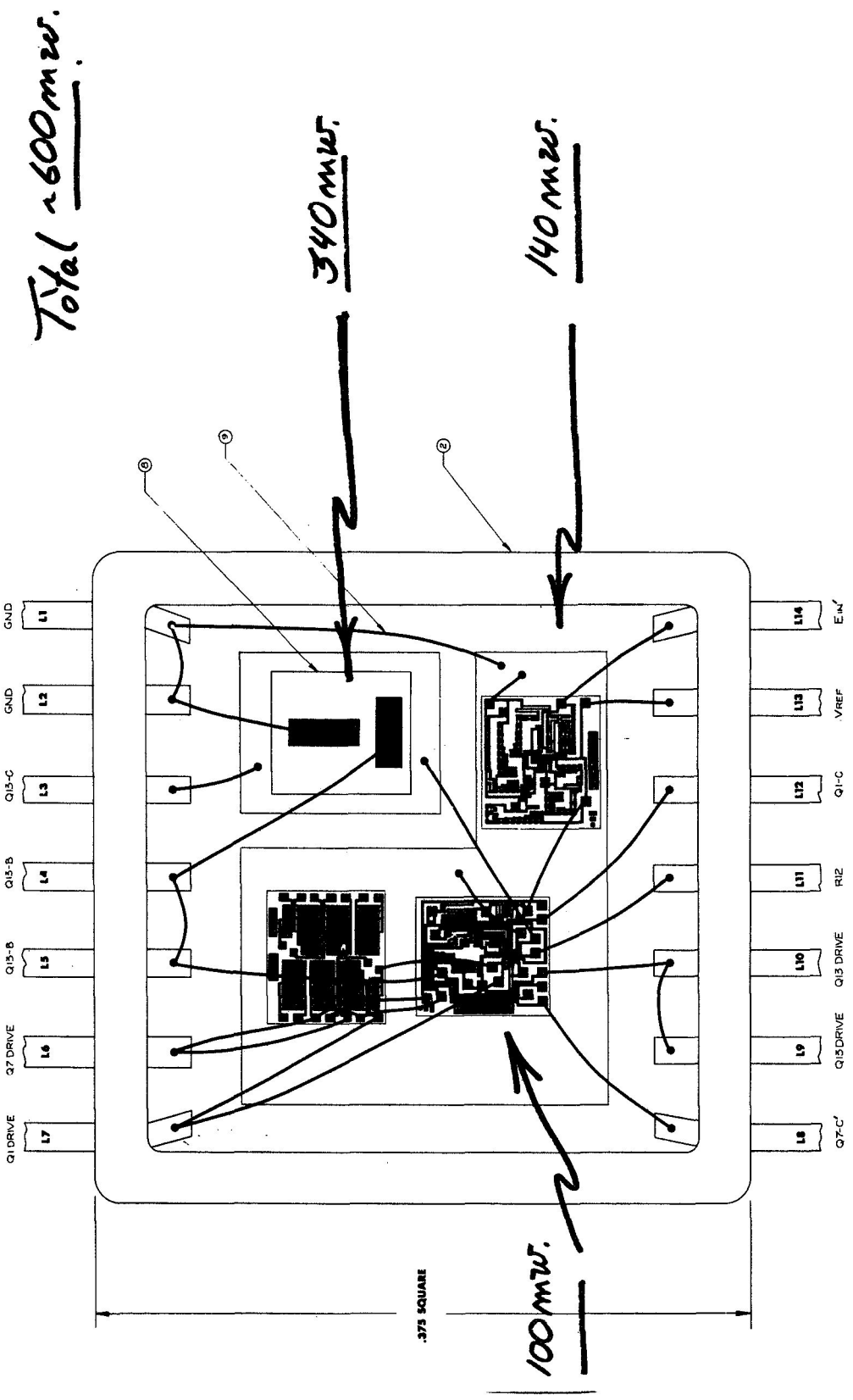
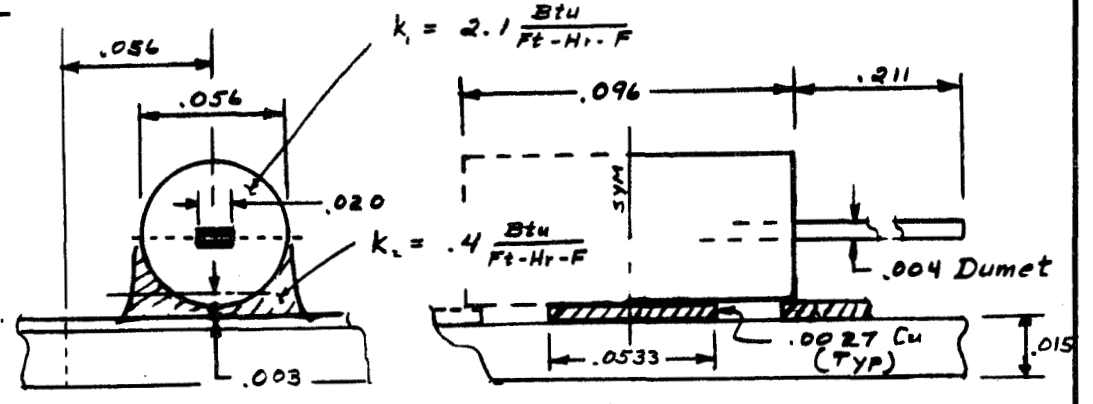


Figure D-2. Flat Package Heat Levels

TRW SYSTEMS		PREPARED BY: H. Lung
PROJECT	SUBJECT	DATE

CR 1



Assume an average gap of .003" between the case and the copper; diode is bonded to board with "Truecast".

Effective Area, $A_e = .866 \times .056 \times .096$

$$A_e = .00465 \text{ in}^2$$

$$R_1 = \frac{l_1}{k_1 A_e} = \frac{.028 \times 12}{2.1 \times .00465}$$

$$R_1 = 34.4 \frac{F}{Btu/Hr}.$$

$$R_2 = \frac{l_2}{k_2 A_2} = \frac{.003 \times 12}{.4 \times .056 \times .096}$$

$$R_2 = 16.8 \frac{F}{Btu/Hr}.$$

Case Resistance :

$$R_c = R_1 + R_2 = 51.2 \frac{F}{Btu/Hr}.$$

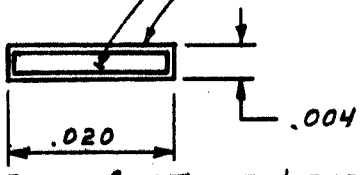
SYSTEMS 1489 REV. 6-65

TRW SYSTEMS		PREPARED BY:
PROJECT	SUBJECT	DATE

$k = 7.26 \frac{Btu}{Hr\text{-}Ft\text{-}F}$

75% (42% Ni, 58% Fe)

25% Cu $k = 220 \frac{Btu}{Hr\cdot Ft\text{-}F}$.



CROSS SECT. OF LEAD

$A = .020 \times .004 = .00008 in^2$

$$R_3 = \frac{.211 \times 12}{7.26 \times .75 \times .00008} = 5810 \frac{F}{Btu/Hr}.$$

$$R_4 = \frac{.211 \times 12}{220 \times .25 \times .00008} = 575 \frac{F}{Btu/Hr}.$$

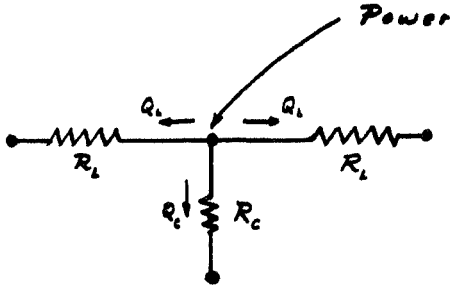
Lead Resistance :

$$R_L = \frac{R_1 R_2}{R_1 + R_2} = 524 \frac{F}{Btu/Hr}.$$

Calculated Conductivity of Dumet with pure copper :

$k = 60 \frac{Btu}{Hr\text{-}Ft\text{-}F}$.

SYSTEMS 1489 REV. 8-65



① $2Q_L + Q_c = Q_T$

② $Q_L R_L = Q_c R_c$

Substituting ① into ②:

$$Q_L R_L = (Q_T - 2Q_L) R_c$$

$$Q_L = \frac{Q_T R_c}{R_L + 2R_c}$$

$$Q_L = \frac{.477 \times 51.2}{524 + (2 \times 51.2)}$$

$$Q_L = .039 \text{ Btu/Hr.}$$

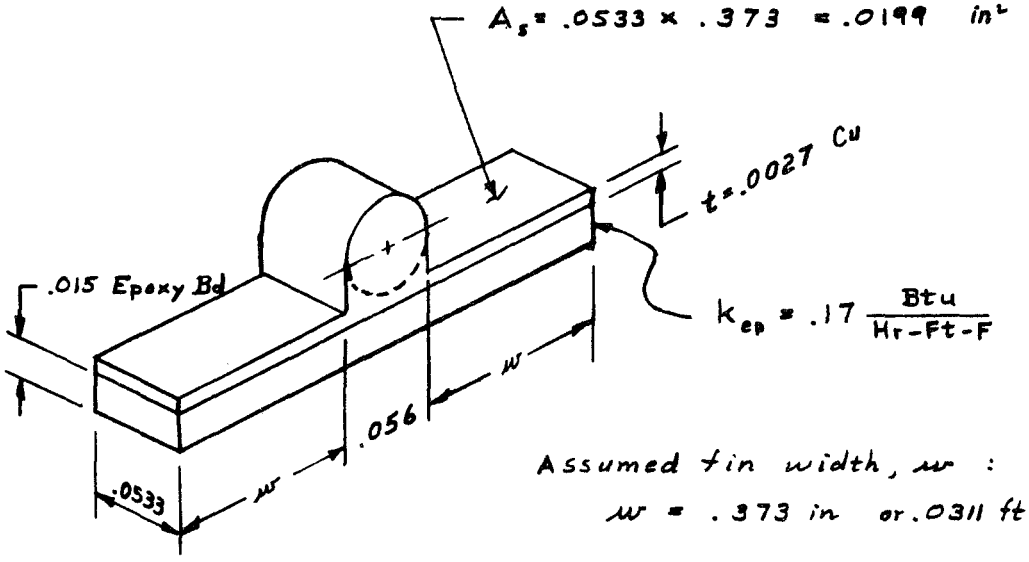
$$Q_c = .477 - 2Q_L$$

$$Q_c = .40 \text{ Btu/Hr.}$$

Temp. Drop across the diode case is assumed equal to the ΔT through each of the two Dumet leads.

$$\Delta T_1 = Q_L R_L = Q_c R_c$$

$$\Delta T_1 = .40 \times 51.2 = 20.5 \text{ F.}$$



Assumed fin width, w :

w = .373 in or .0311 ft

For constant heat flux through the epoxy bd. & copper:

$$R = \frac{.0027 \times 12}{226 \times .0199} + \frac{.015 \times 12}{.17 \times .0199} = .0072 + 53.2$$

$$R = 53.2 \ \frac{F}{Btu/Hr} .$$

$$h = \frac{1}{RA_s} = \frac{144}{53.2 \times .0199}$$

$$h = 136 \ \frac{Btu}{Hr-Ft^2-F} .$$

Fin efficiency :

Ref (1)

$$\eta = \frac{\tanh w\sqrt{\frac{h}{kt}}}{w\sqrt{\frac{h}{kt}}}$$

$$w\sqrt{\frac{h}{kt}} = .0311\sqrt{\frac{136}{226 \times .000225}} = 1.61$$

$$\eta = \frac{\tanh 1.61}{1.61} = \frac{.92316}{1.61}$$

$$\eta = 57.3\ \%$$

Equivalent fin size with same temp. as root temp.

$A_p = .373 \times .0533 = .0199\ in^2$

$57.3\%\ A_p = .0114\ in^2$

Equiv. width, w_e

$$w_e = \frac{.0114}{.053} = .215\ in.$$

Equiv. surface area of constant temp.

$[(2 \times .215) + .056].0533 = .0259\ in^2$

Actual Resistance across the epoxy bd. & copper:

$$R = \frac{.0027 \times 12}{226 \times .0259} + \frac{.015 \times 12}{.17 \times .0259} = 40.8\ \frac{F}{Btu/Hr}.$$

$Q_c = .40\ Btu/Hr$

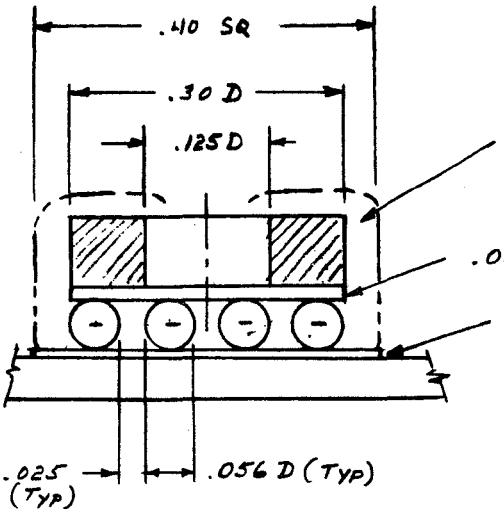
$\Delta T_2 = Q_c R = 16.4\ F.$

Total temp rise from jct. pt. of CR-1 to Alum. TB:

$\Delta T_T = \Delta T_1 + \Delta T_2 = 20.5 + 16.4$

$\Delta T_T = 36.9\ F.$ or $20.5\ C.$

XFMR



Transformer Core Resistance is combined resistances along 3 thermal paths.

R_1 is thru mylar and diode.

R_2 is thru mylar and "Truecast" (between diodes).

R_3 is thru "Truecast" (via periphery).

Path 1 (to ctr of diode):

$$R_1 = \sum \frac{l}{kA} = \frac{.005 \times 12}{.087 \times .056 \times .096} + \frac{.028 \times 12}{2.1 \times .00465}$$

$$+ \frac{.010 \times 12}{.40 \times .056 \times .096} \quad \text{(Note: for 1/2 path)}$$

$$R_1 = \tfrac{1}{2}(128.4 + 34.4 + 55.8) = 109.3 \ \frac{F}{Btu/Hr}.$$

Path 1' (ctr of diode to alum. base):

$$R_1' = \frac{.028 \times 12}{2.1 \times .00465} + \frac{.010 \times 12}{.40 \times .056 \times .096} + \frac{.003 \times 12}{.10 \times .056 \times .096}$$

$$R_1' = 157.2 \ \frac{F}{Btu/Hr}. \quad \text{(Note: for 1/2 path)}$$

$$R_1' = 78.6 \ \frac{F}{Btu/Hr}.$$

Path 2 :

Effective Area, $A = .785(D_o^2 - D_i^2) - 2(.056 \times .096)$

$A = .0584 - .01075 = .0476\ in^2$

$$R_2 = \sum \frac{1}{kA} = \frac{.005 \times 12}{.087 \times .0476} + \frac{.056 \times 12}{.40 \times .0476} + \frac{.003 \times 12}{.10 \times .0476}$$

$R_2 = 14.5 + 35.2 + 7.56$

$R_2 = 57.3 \frac{F}{Btu/Hr}$.

Path 3 :

$A_1 = \pi(.40)(.0875) = .11\ in^2$

$A_2 = (.40)^2 - .785(.30)^2 = .09\ in^2$

$$R_3 = \frac{.05 \times 12}{.40 \times .11} + \frac{.105 \times 12}{.40 \times .09} + \frac{.003 \times 12}{.10 \times .09}$$

$R_3 = 13.6 + 35.0 + 4.0$

$R_3 = 52.6 \frac{F}{Btu/Hr}$.

Combining Resistances, R_2 & R_3 into R_4 :

$$R_4 = \frac{R_2 R_3}{R_2 + R_3} = \frac{3020}{109.9} = 27.5 \frac{F}{Btu/Hr}.$$

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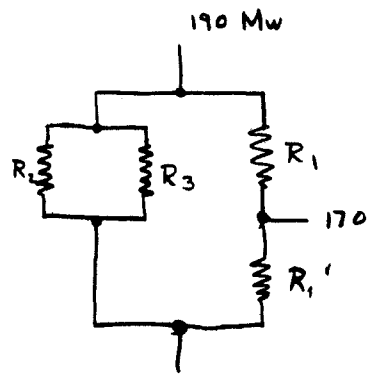
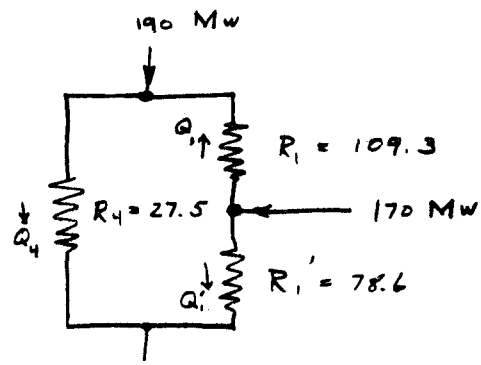


Equiv. Circuit



Modified Circuit

Using Modified Circuit :

$$Q_1' R_1' = Q_1 R_1 + (Q_1 + 190) R_4$$

$$Q_1' + Q = 170 \quad \text{or} \quad Q_1' = 170 - Q_1$$

$$(170 - Q_1) R_1' = Q_1 R_1 + Q_1 R_4 + 190 R_4$$

$$Q_1 = \frac{170 R_1' - 190 R_4}{R_1 + R_4 + R_1'} = \frac{170 \times 78.6 - 190 \times 27.5}{109.3 + 27.5 + 78.6}$$

$Q_1 = 37.8$ Mw or .13 Btu/Hr.

$Q_1' = 170 - 37.8 = 132.2$ Mw or .45 Btu/Hr

$Q_4 = Q_1 + 190 = 227.8$ Mw or .776 Btu/Hr

$\Delta T_1' = R_1' Q_1' = 78.6 \times .45 = 35.4$ F (19.6 C)

$\Delta T_4 = R_4 Q_4 = 27.5 \times .776 = 21.4$ F (11.9 C)

$\Delta T_1 = R_1 Q_1 = 109.3 \times .13 = 14.2$ F (7.9 C)

∴ Junction temp. of diode is :

$\Delta T_1' = 35.4$ F. or 19.6 C.

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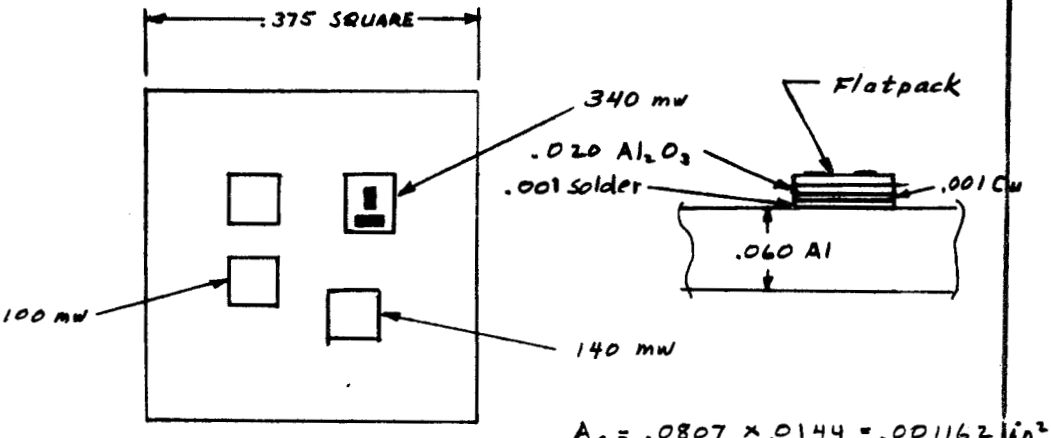
FLATPACK



$A_c = .0807 \times .0144 = .001162 \text{ in}^2$

$k_{Al_2O_3} = 10.7 \frac{Btu}{Hr\text{-}Ft\text{-}F}$.

$k_{solder} = 14$ " .

$k_{cu} = 222$ " .

Typical Resistance per flatpack:

$$R = \sum \frac{l}{kA_c} = \frac{12}{.001162}\left(\frac{.020}{10.7} + \frac{.001}{222} + \frac{.001}{14}\right)$$

$R = 2.66 \frac{F}{Btu/Hr}$.

$Q = .340 \times 3.413 = 1.16 \text{ Btu/Hr}$

$\Delta T = QR = 3.1$ F. or 1.7 C.

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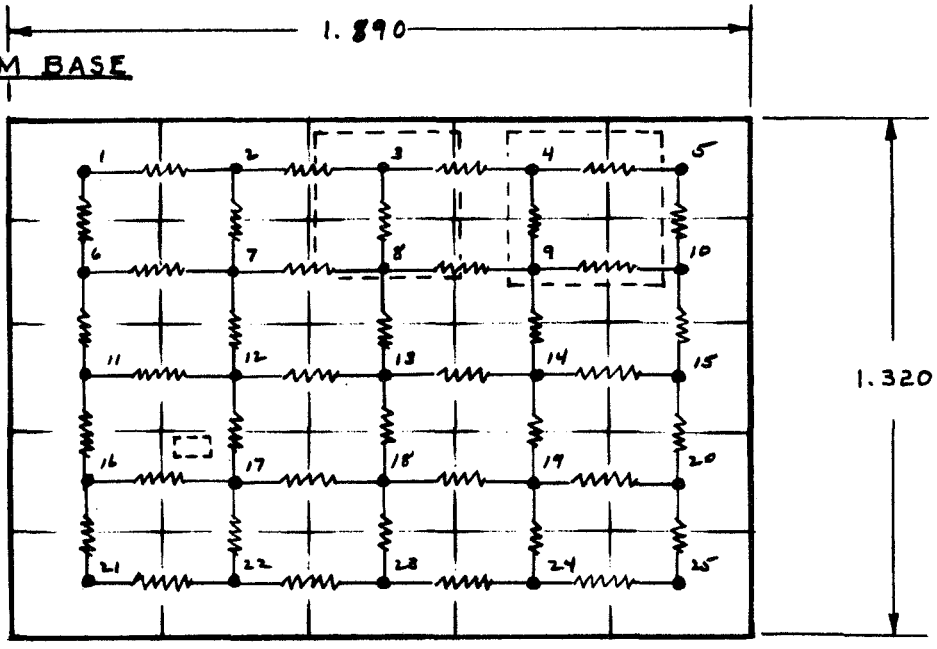
ALUMINUM BASE



Conductances, Resistances:

1-2, 2-3, 3-4, 4-5, 6-7, 7-8, 8-9, 9-10, 11-12, 12-13, 13-14, 14-15, 16-17, 17-18, 18-19, 19-20, 21-22, 22-23, 23-24, 24-25

(across) $K = \frac{kA}{l} = \frac{100 \times .06 \times .364}{12 \times .378} = .35$ Btu/Hr-F.

$R = K^{-1} = 2.86 \frac{F-Hr}{Btu}$.

1-6, 6-11, 11-16, 16-21, 2-7, 7-12, 12-17, 17-22, 3-8, 8-13, 13-18, 18-23, 4-9, 9-14, 14-19, 19-24, 5-10, 10-15, 15-20, 20-25

(down) $K = \frac{100 \times .06 \times .378}{12 \times .264} = .716$ Btu/Hr-F.

$R = 1.397 \frac{F-Hr}{Btu}$.

Heat Input:

Node 3 $Q_3 = .340 \times 3.413 = 1.16$ Btu/Hr.

Node 8 $Q_8 = .260 \times 3.413 = .887$ " .

Node 4 $Q_4 = 3/5 (.2 \times 3.413) = .41$ " .

Node 9 $Q_9 = 3/5 (.2 \times 3.413) = .41$ " .

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Node 5 $Q_5 = 2/5(.2 \times 3.413) = .273$ Btu/Hr.

Node 10 $Q_{10} = 2/5(.2 \times 3.413) = .273$ "

Node 17 $Q_{17} = .14 \times 3.413 = .477$ "

Interface Resistance:

Assume interface conductivity

$$h = 200 \frac{\text{Btu}}{\text{Hr-Ft}^2\text{-F}}.$$

$$R = \frac{1}{hA} = \frac{144}{200 \times .264 \times .378}$$

$$R = 7.2 \frac{\text{F}}{\text{Btu/Hr}}.$$

Subsequent table of node temperatures were obtained from a Thermal Circuit Analyzer.

Temperature Rise of Nodes from Infinite Heat Sink

Node	ΔT (F)	Node	ΔT (F)
1	.8	13	1.2
2	1.2	14	1.1
3	2.4	15	1.1
4	2.0	16	.3
5	1.7	17	.8
6	.7	18	.8
7	1.0	19	.8
8	2.0	20	.8
9	1.7	21	0
10	1.5	22	.5
11	.5	23	.7
12	.9	24	.7
		25	.7

Max. temp. rise for CR-1 :

$\Delta T = 36.9 + .8 = 37.7$ F.

$\Delta T = 20.9$ C.

Max. temp. rise for flatpack:

$\Delta T = 3.1 + 2.4 = 5.5$ F.

$\Delta T = 3.1$ C.

Max. temp. rise for Xfmr :

$\Delta T = 35.4 + 1.7 = 37.1$ F.

$\Delta T = 20.6$ C.

References :

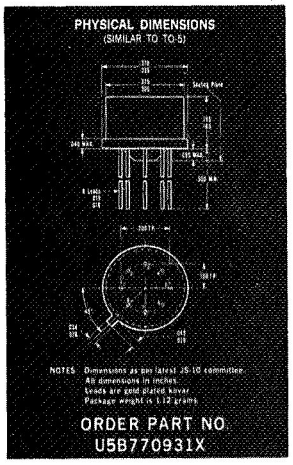
(1) "Conduction Heat Transfer", P. J. Schneider, Addison - Wesley, 1957, p. 73.

APPENDIX E

FAIRCHILD μA709 AMPLIFIER DATA SHEETS

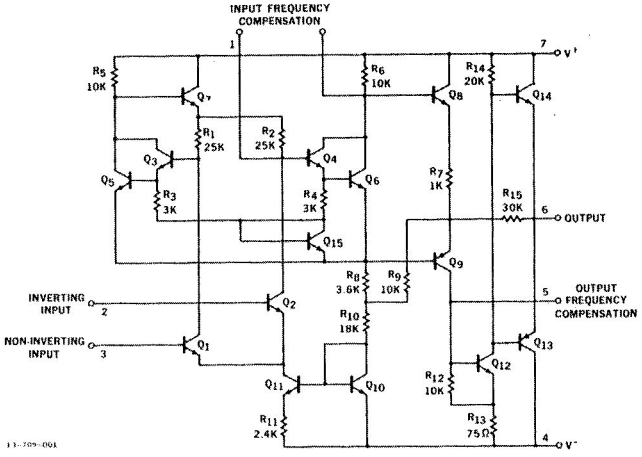
μA709
HIGH PERFORMANCE OPERATIONAL AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

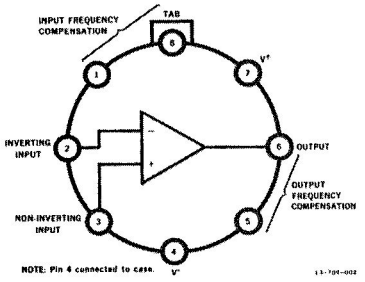
GENERAL DESCRIPTION - The μA709 is a High-Gain Operational amplifier constructed on a single silicon chip using the Fairchild Planar epitaxial process. It features low offset, high input impedance, large input common mode range, high output swing under load and low power consumption. The device displays exceptional temperature stability and will operate over a wide range of supply voltages with little degradation of performance. The amplifier is intended for use in DC servo systems, high impedance analog computers, in low-level instrumentation applications and for the generation of special linear and nonlinear transfer functions.



ABSOLUTE MAXIMUM RATINGS

Supply Voltage		± 18 Volts
Internal Power Dissipation	(Note 1)	300 mW
Differential Input Voltage		± 5.0 Volts
Input Voltage		± 10 Volts
Output Short-Circuit Duration	(T_A = 25°C)	5 sec
Storage Temperature Range		-65°C to + 150°C
Operating Ambient Temperature Range		-55°C to + 125°C
Lead Temperature (Soldering, 60 sec)		300°C





CONNECTION DIAGRAM
(TOP VIEW)

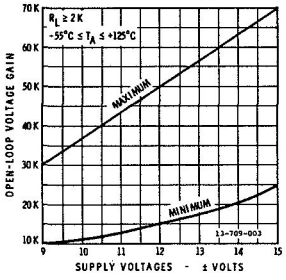
NOTE 1: Rating applies for case temperatures to + 125°C; derate linearly at 5.6 mW/°C for ambient temperatures above + 95°C.

ELECTRICAL CHARACTERISTICS (T_A = +25°C, ±9 V ≤ V_S ≤ ±15 V Unless Otherwise Noted)

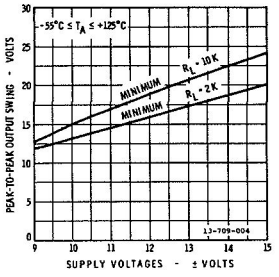
Parameter (See definitions)	Conditions	Min.	Typ.	Max.	Units
Input Offset Voltage	$R_S \leq 10$ K		1.0	5.0	mV
Input Offset Current			50	200	nA
Input Bias Current			200	500	nA
Input Resistance		150	400		KΩ
Output Resistance			150		Ω
Power Consumption	V_S = ±15 V		80	165	mW
The following specifications apply for -55°C ≤ T_A ≤ +125°C:					
Input Offset Voltage	$R_S \leq 10$ K			6.0	mV
Average Temperature Coefficient of Input Offset Voltage	R_S = 50 Ω		3.0		μV/°C
	$R_S \leq 10$ K		6.0		μV/°C
Large-Signal Voltage Gain	V_S = ±15 V, $R_L \geq 2$ K, V_{OUT} = ±10 V	25,000	45,000	70,000	
Output Voltage Swing	V_S = ±15 V, $R_L \geq 10$ K	±12	±14		V
	V_S = ±15 V, $R_L \geq 2$ K	±10	±13		V
Input Voltage Range	V_S = ±15 V	±8.0	±10		V
Common Mode Rejection Ratio	$R_S \leq 10$ K	70	90		db
Supply Voltage Rejection Ratio	$R_S \leq 10$ K		25	150	μV/V
Input Offset Current	T_A = +125°C		20	200	nA
Input Offset Current	T_A = -55°C		100	500	nA
Input Bias Current	T_A = -55°C		0.5	1.5	μA

GUARANTEED ELECTRICAL CHARACTERISTICS

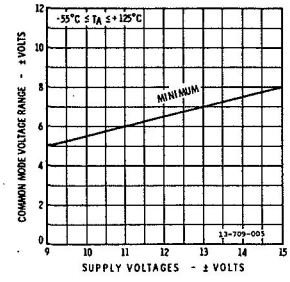
VOLTAGE GAIN



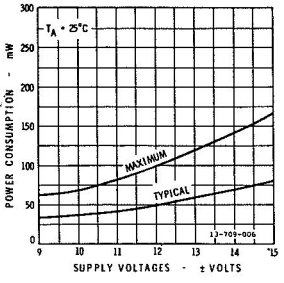
OUTPUT SWING



INPUT COMMON MODE VOLTAGE RANGE

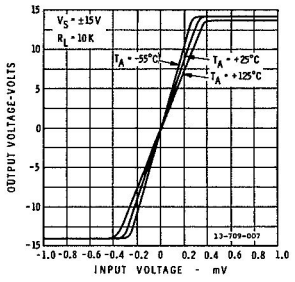


POWER CONSUMPTION

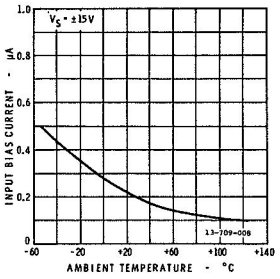


TYPICAL PERFORMANCE CURVES

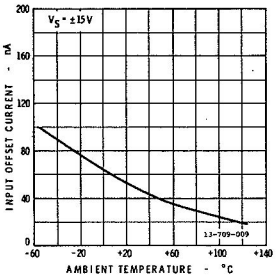
VOLTAGE TRANSFER CHARACTERISTIC



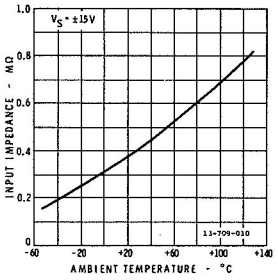
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



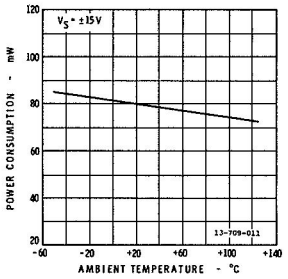
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



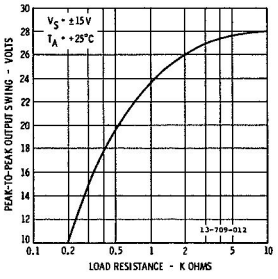
INPUT IMPEDANCE AS A FUNCTION OF AMBIENT TEMPERATURE



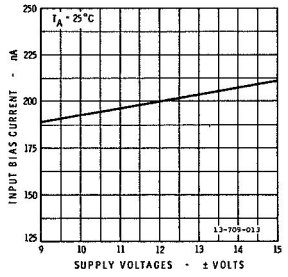
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



PEAK OUTPUT SWING AS A FUNCTION OF LOAD RESISTANCE



INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



DEFINITION OF TERMS

INPUT OFFSET VOLTAGE - That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT - The difference in the currents into the two input terminals with the output at zero volts.

INPUT RESISTANCE - The resistance looking into either input terminal with the other grounded.

INPUT BIAS CURRENT - The average of the two input currents.

INPUT VOLTAGE RANGE - A range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

INPUT COMMON MODE REJECTION RATIO - The ratio of the input voltage range to the maximum change in input offset voltage over this range.

LARGE-SIGNAL VOLTAGE GAIN - The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT VOLTAGE SWING - The peak output swing, referred to zero, that can be obtained without clipping.

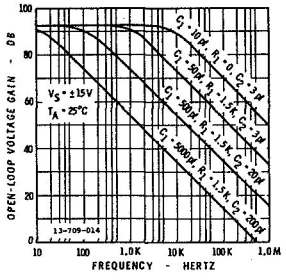
OUTPUT RESISTANCE - The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

POWER CONSUMPTION - The DC power required to operate the amplifier with the output at zero and with no load current.

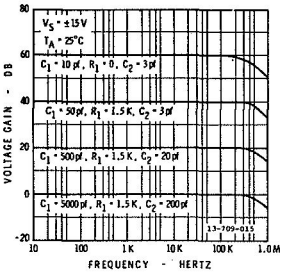
SUPPLY VOLTAGE REJECTION RATIO - The ratio of the change in input offset voltage to the change in supply voltage producing it.

TYPICAL PERFORMANCE CURVES

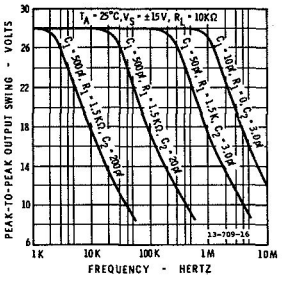
OPEN-LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF COMPENSATION



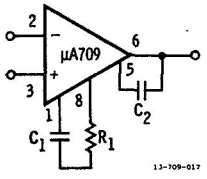
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS



MAXIMUM OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS COMPENSATION NETWORKS



FREQUENCY COMPENSATION CIRCUIT



APPENDIX F

MULTI-CIRCUIT DIE PHILOSOPHY

APPENDIX F

MULTI-CIRCUIT DIE PHILOSOPHY

The Multi-Circuit Die of TRW Systems is a means of expediently supplying a fully integrated circuit at minimum cost. It is an active substrate containing twelve transistor structures. Thin film resistors and an aluminum interconnection pattern convert this transistor array into a fully integrated circuit as shown in Figure F-1.

The advantages of this approach are realized because one basic semiconductor substrate is processed and stockpiled independent of a circuit requirement. The largest proportion of total processing time is taken to fabricate the semiconductor substrates (five primary processing steps and four masks). These MCD wafers are then ready and waiting to be committed to a specific circuit. Circuit fabrication is completed by using four additional masks which interconnect the transistors with resistors in a prescribed pattern. Lead time is consequently decreased to about one month (the time required to fabricate the four masks and process the four steps). Table F-I indicates the patterns needed to make a complete integrated circuit.

This approach is particularly attractive for small or medium quantities of circuits (10 to 100) since the cost and time factors would usually outweigh the restrictions of a common substrate (for instance, circuit flexibility and using one type of transistor). Large quantities (100 and up) could economically justify special semiconductor substrates for each circuit, in that the yield could often be increased by structuring each transistor according to its particular application in the circuit.

The transistor structure chosen should meet the needs of the majority of circuit applications because it is constructed with the smallest lateral geometries consistent with good fabrication yield. This minimum geometry device provides excellent high frequency performance (high f_t at low current levels, together with low junction capacitances) and maintains high betas at very low current levels. These minimum geometry transistors can be paralleled when large currents are required, thereby retaining excellent high frequency performance. The MCD substrates are

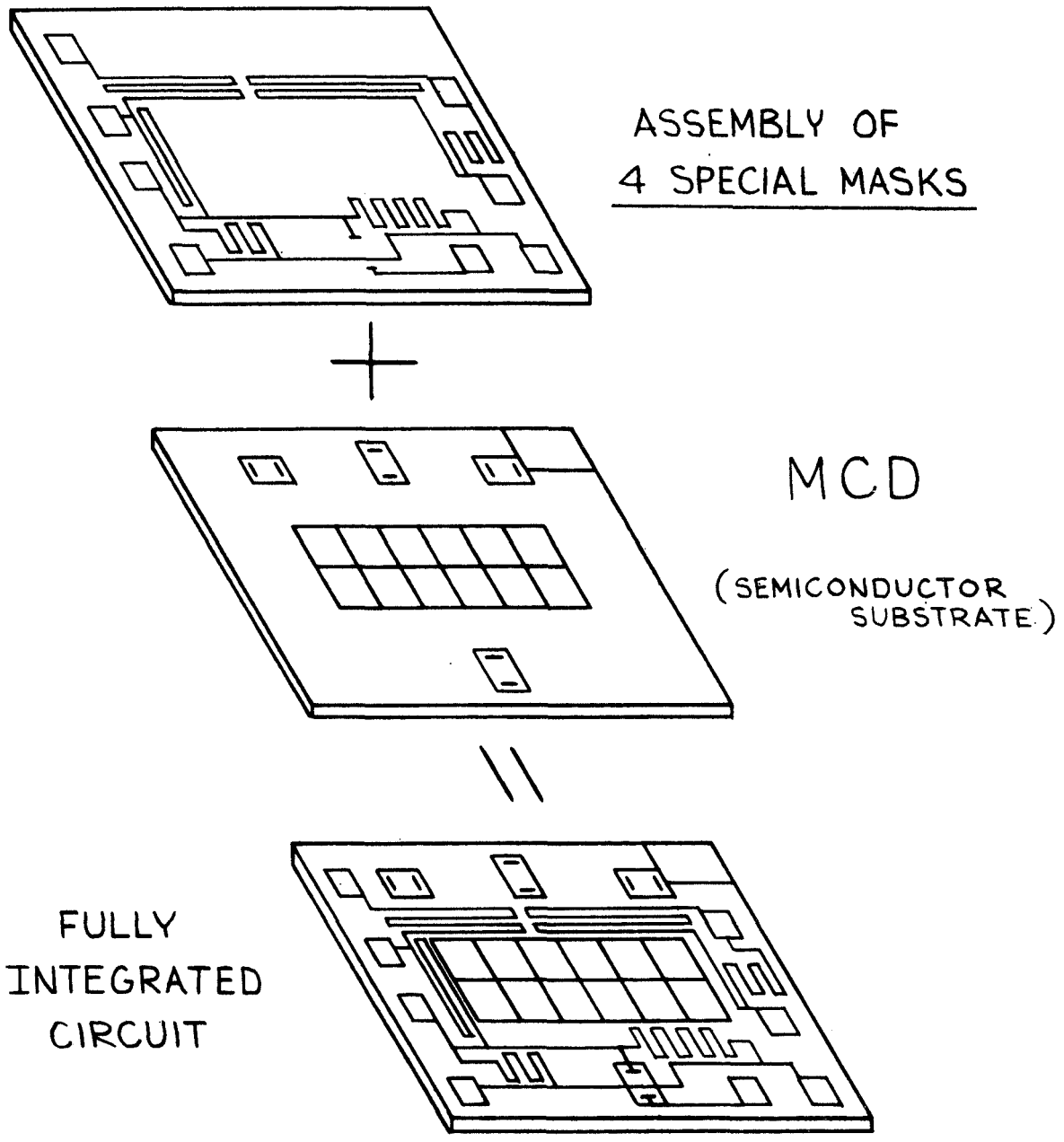


Figure F-1. Multi-Circuit Die Assembly Philosophy

selected so the designer can choose from a given distribution of betas and breakdown voltages.

The MCD basic substrate is shown in Figure F-2. All of the transistors are located in the center of the die to maximize parameter matching. (The probability is high that any two adjacent transistors are well matched.) The clear area around the transistor cluster is available for resistors, interconnections, and bonding pads as shown in the metallization pattern of Figure F-3. Crossunders are provided specifically in four locations and generally in any of the transistor positions. (A transistor can be used as a transistor, diode, capacitor, or crossunder, as determined by the placement of the contact holes in the oxide, aluminum interconnection, and application of the circuit.)

Figures F-4 through F-7 show typical circuits and the associated schematics which were fabricated from the MCD1 substrate.

TABLE F-I. PATTERNS NEEDED FOR INTEGRATED CIRCUIT FABRICATION

BLE	DI
1. Buried Layer Pattern	1. Dielectric Isolation Etch Pattern
2. Epitaxy Isolation Pattern	2. Base Pattern
3. Base Pattern	3. Emitter Pattern
4. Emitter Pattern	
STOCKPILE	
5. Contact Pattern	(To place holes in oxide to make contact with resistors)
6. Cermet Pattern	(Thin film resistance definition)
7. Second Metal Pattern	(Interconnect Devices)
FINISHED CIRCUIT	

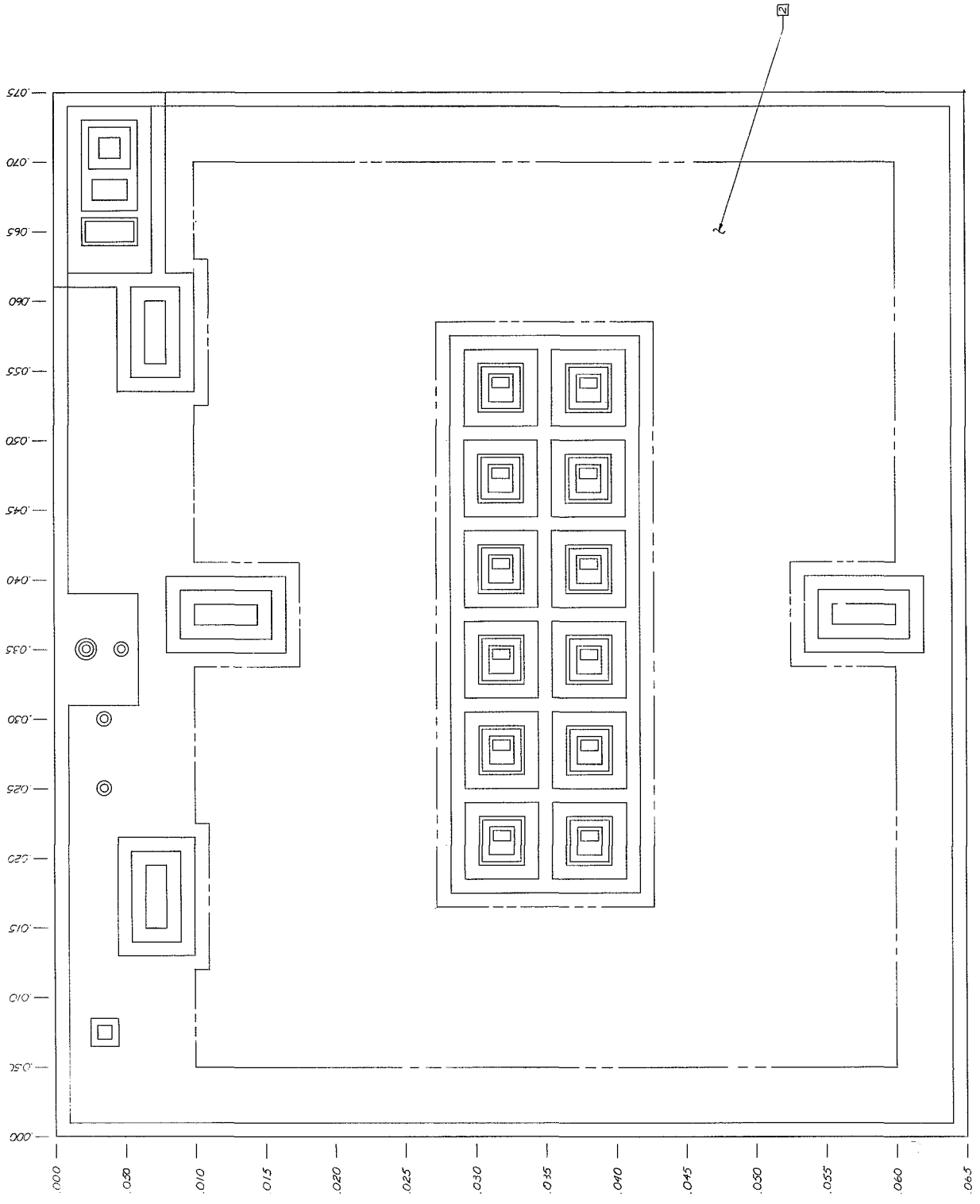


Figure F-2. Multi-Circuit Die Basic Substrate

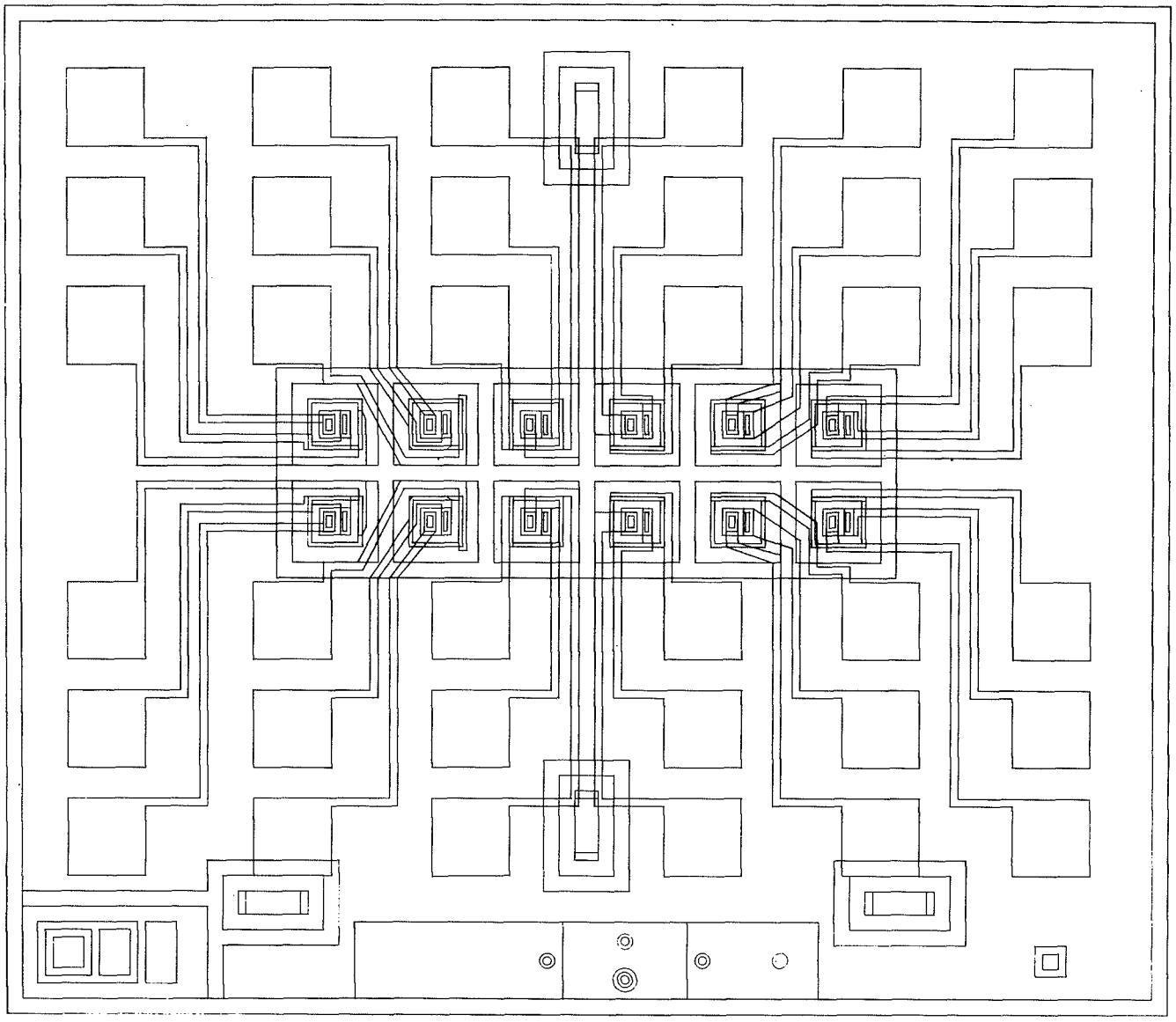


Figure F-3. Multi-Circuit Die Metallization Pattern

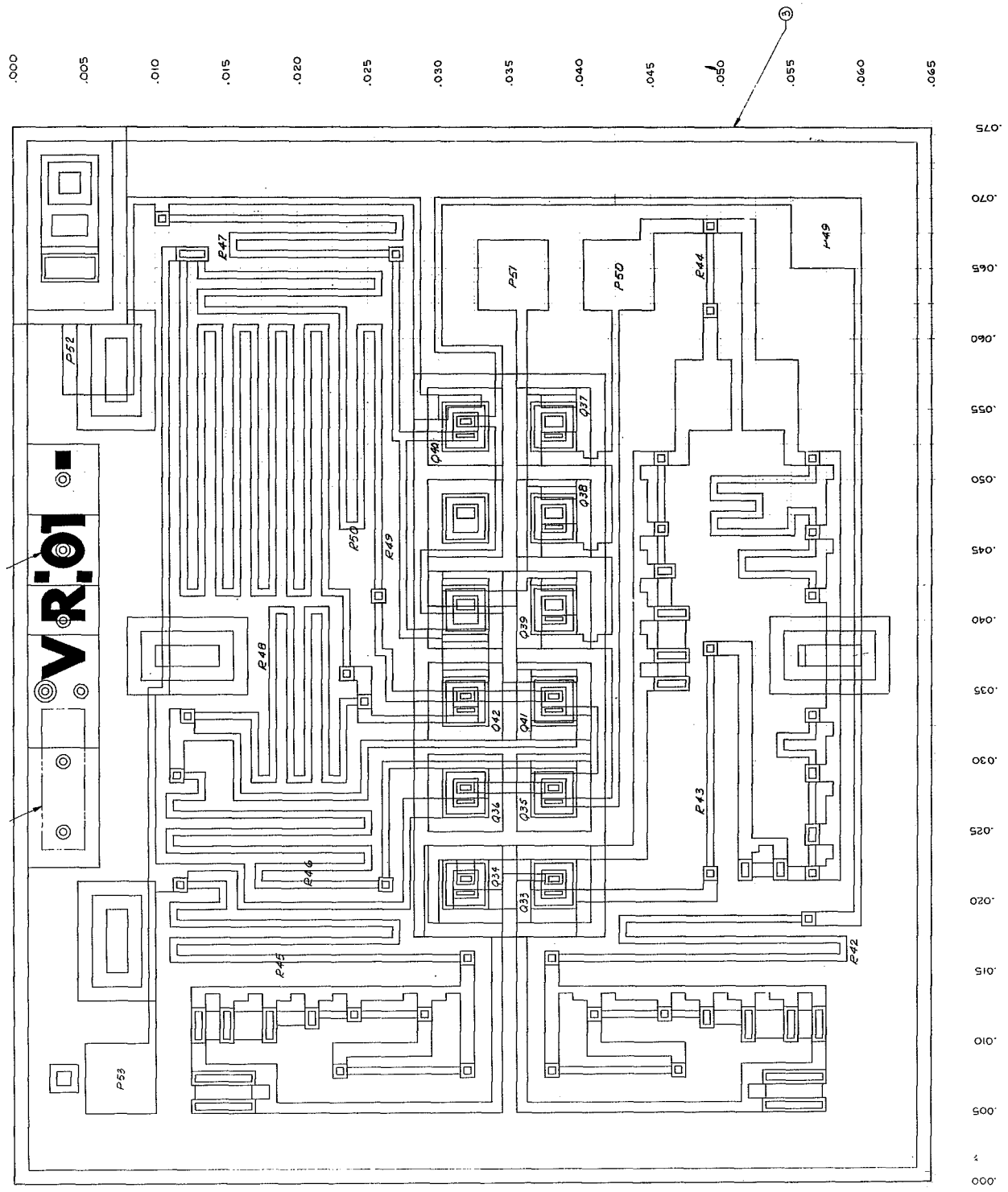


Figure F-4. Multi-Circuit Die Voltage Regulator (VR-01) Drawing

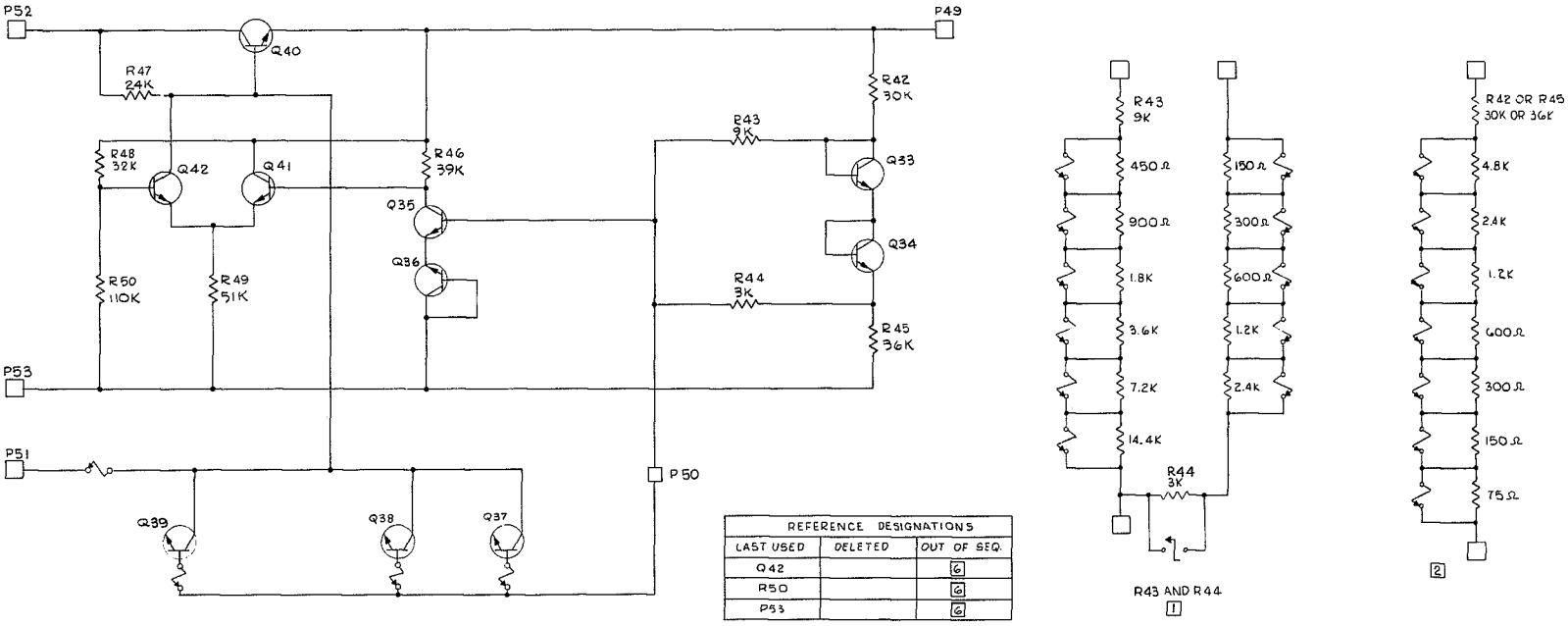


Figure F-5. Multi-Circuit Die Voltage Regulator (VR-01) Schematic

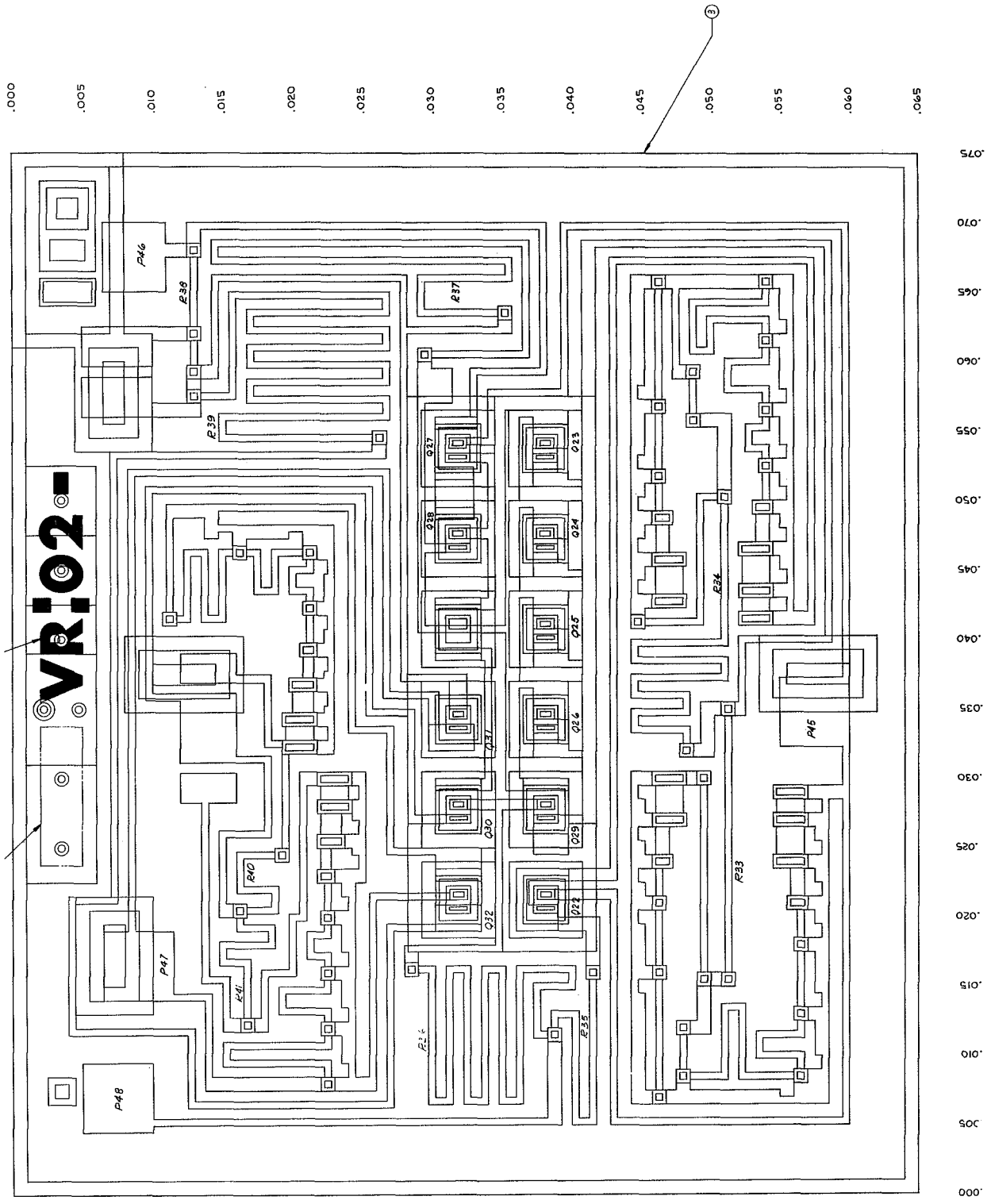


Figure F-6. Multi-Circuit Die Voltage Regulator (VR-02) Drawing

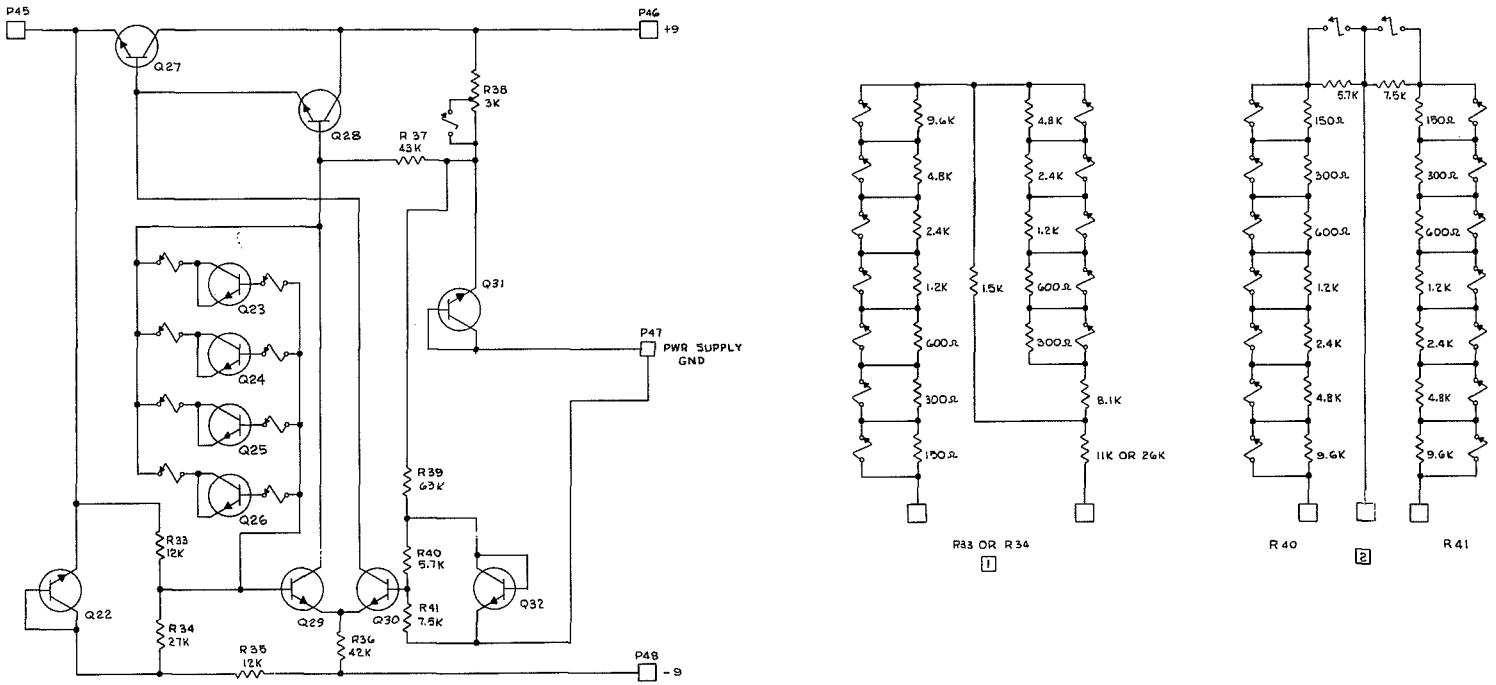


Figure F-7. Multi-Circuit Die Voltage Regulator (VR-02) Schematic

APPENDIX G

FAIRCHILD LDDTμL 9040, 9041, AND 9042; DTμL 933; AND DTμL 946 DIODE-TRANSISTOR MICROLOGIC DATA SHEETS

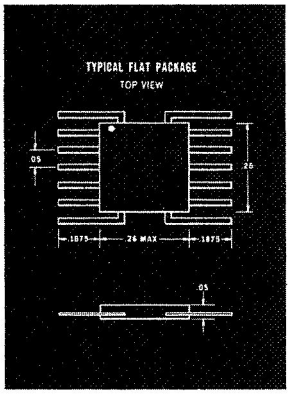
DTμL 946
QUAD TWO-INPUT GATE ELEMENT
FAIRCHILD DIODE-TRANSISTOR MICROLOGIC

The DTμL 946 Element consists of four 2-Input Gates on a monolithic chip. The circuit design and fabrication technology are matched identically to the DTμL 930 Dual 4-Input Gate Element and to the DTμL family in general.

The logic gating sections of a computer or data handling system may be economically generated from the DTμL family with these elements:

DTμL 946	Quad 2-Input Gate Element—inverters, exclusive "OR's", fan-in 2 gates.
DTμL 930	Dual 4-Input Gate Element—higher fan-in gating (with input extension available in each gate).
DTμL 933	Dual 4-Input Extender Element—for fan-in extending.
DTμL 932	Dual Buffer Element—for high fan-out, good capacitive drive capability, and interface driving. The 932 fan-in may also be increased by use of 933 Elements.

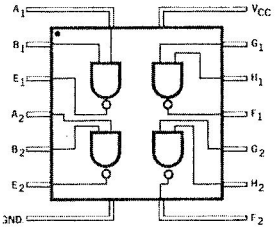
Refer to the DTμL 931 Clocked Flip-Flop Element Specification for the storage function and to the DTμL Composite Specification for complete test data and additional characteristic data.



PART NO. 9194651

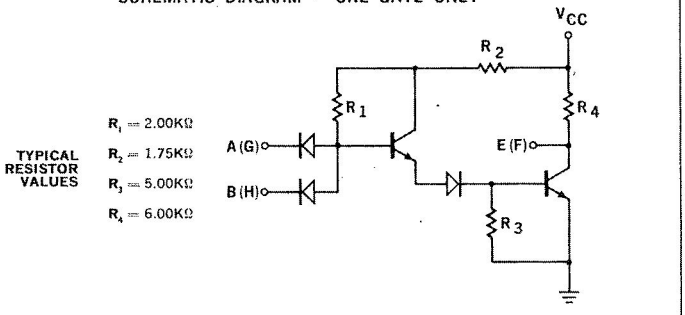
LOGIC DIAGRAM

TYPICAL FLAT PACKAGE



Top View

SCHEMATIC DIAGRAM — ONE GATE ONLY

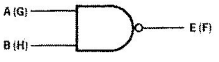


TYPICAL RESISTOR VALUES

$R_1 = 2.00K\Omega$
$R_2 = 1.75K\Omega$
$R_3 = 5.00K\Omega$
$R_4 = 6.00K\Omega$

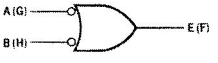
POSITIVE (NAND) LOGIC

$E = \overline{A \cdot B}$
$F = \overline{G \cdot H}$



NEGATIVE (NOR) LOGIC

$E = \overline{A + B}$
$F = \overline{G + H}$



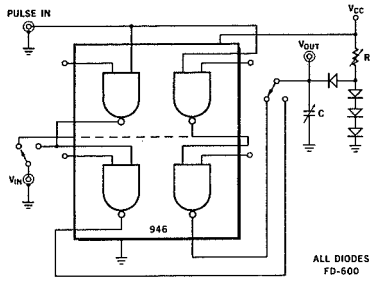
313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA
FAIRCHILD SEMICONDUCTOR

TEST SPECIFICATIONS AND CHARACTERISTIC CURVES

CHARACTERISTICS - All curves and other data shown in the DTμL 930 Element specifications and in the DTμL Composite specifications apply equally to each gate on the DTμL 946 Element, except as it may be necessary to modify test circuits to fit the proper pin configurations.

TEST SPECIFICATIONS - The test sequence for the DTμL 930 Element, shown on Page 2 of the DTμL Composite Specification, and the various tables of test conditions, test limits, LTPD's, and t_{switch} conditions from Pages 3 and 5 also apply to the 946 Element, except as modified below:

1. Test limits for I_{PDH} and I(max) are twice 930 values on the 946.
2. Ignore all tests relating to pins C, D, I, J, X, and Y.
3. Tests 1, 3, 4, 7, 8, 11, 13, 19, 21, 27, and 29 are made on the $A_1 B_1 E_1$ gate; then repeated on the $A_2 B_2 E_2$ gate; then the matching tests made on the $G_2 H_2 F_2$ and $G_1 H_1 F_1$ gates.
4. The following t_{pd} test circuit is used:

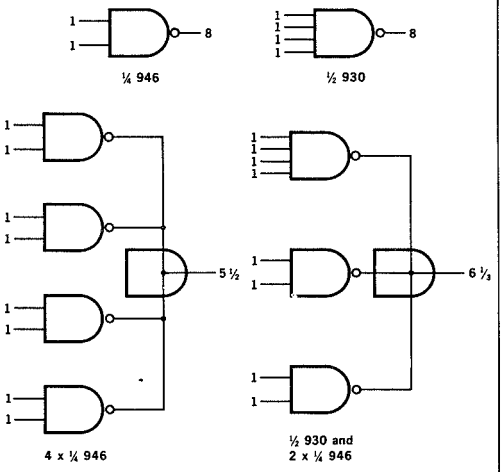


APPLICATIONS OF THE QUAD 2-INPUT GATE

Most of the advantages in reducing element count and assembly cost by having four 2-Input gates in one package are obvious. Considering the large percentage of occurrences of fan-in 1 and 2 in the typical system, savings of 50% of elements needed to accomplish the fan-in 1 and 2 gating is substantial. However, some logic manipulation using the output "OR"ing capability may lead to yet greater savings. Thus, it is a further advantage of Fairchild Diode-Transistor μLogic that the gates (DTμL 930 Dual 4-Input Gate Element and DTμL 946 Quad 2-Input Gate Element) may be output "OR"ed with fractional fan-out subtraction and without a separate gate with open collector required.

The example below, a 2-element full adder, shows the typical use of the Quad 2-Input Gate in an optimized logic configuration.

Suggested Loading Rules DTμL 930 and 946 (see DTμL Composite for more complete rules and tradeoffs) are shown at right.



DESIGN OF A BINARY FULL ADDER

The classical Binary Full Adder is often decomposed into two half-adder circuits for reasons of economy. Such a mechanization, while slower, significantly reduces the logic circuitry involved. The arrangement given below accomplishes all of the functions required of a full-adder with only two DTμL 946 elements and introduces a logic delay of only four gate propagation times. All of the signals required for a "carry lookahead" organization are also present.

The rationale for this mechanization derives from the following factorization of the expressions for the full-adder sum (S) and carry (C). Output carry signals are distinguished from the carry input by a prime mark:

$$S = A\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}\bar{B}C + ABC$$
$$= (A\bar{B} + \bar{A}B)\bar{C} + (\bar{A}\bar{B} + AB)C$$
$$C' = A\bar{B}C + \bar{A}BC + AB\bar{C} + ABC$$
$$= (A\bar{B} + \bar{A}B)C + AB(\bar{C} + C)$$
$$= (A\bar{B} + \bar{A}B)C + AB$$

Note also that

$$\overline{(A\bar{B} + \bar{A}B)} = \bar{A}\bar{B} + AB$$

It is apparent that the sum is the exclusive "OR" of the carry input with the result of the exclusive "OR" of the arguments A and B.

Two different exclusive "OR" circuits are used. In the first, composed of NAND Gates 1 and 2, it is assumed that both true and complement values of the arguments are available. The direct connection of the outputs at point X has logical effect; namely, that of ANDing the NAND outputs together.

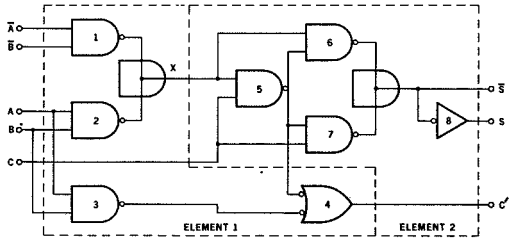
Therefore, $\overline{A\bar{B}} \cdot \overline{\bar{A}\bar{B}} = \overline{A\bar{B} + \bar{A}\bar{B}} = A\bar{B} + \bar{A}B$

The second exclusive "OR", composed of NAND Gates 5, 6, 7, and 8, requires only true inputs, avoiding the need for two inverters at its input.

Both the true and complement sum outputs are obtained by the "wired OR" connection and NAND Gate 8, which is used as an inverter.

The output of NAND Gate 5 is the term $(A\bar{B} + \bar{A}B)C$ with the proper polarity for NOR Gate 4.

The remaining term of the carry originates in NAND Gate 3 with the proper polarity for NOR Gate 4. The output polarity of NOR Gate 4 is correct for a cascaded full-adder.



DTμL933 DUAL FOUR-INPUT EXTENDER ELEMENT

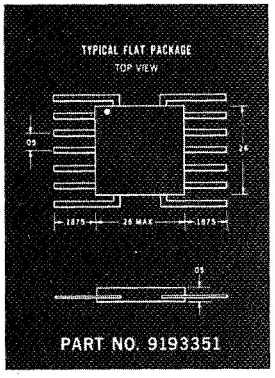
FAIRCHILD DIODE-TRANSISTOR MICROLOGIC

The DTμL 933 is a Dual Input-Extender consisting of two independent diode arrays identical in every respect to the input diodes of the DTμL Gate and Buffer elements. DTμL 933 elements may be used to extend fan-in capability to more than 20 without adversely affecting the noise immunity or load driving capability of the element to which they are connected.

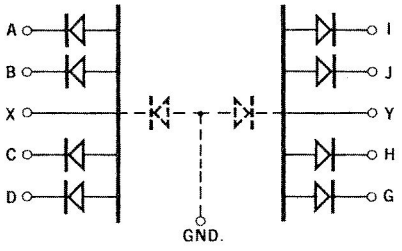
Good practice dictates that extension interconnection paths be as short as possible to minimize the effects of distributed capacitance on circuit performance. The effects of capacitance are summarized on the back page.

Typical input capacitance of DTμL 933 is 2 pf and output capacitance is 5 pf.

For complete test sequence and test values, please refer to the composite DTμL specification

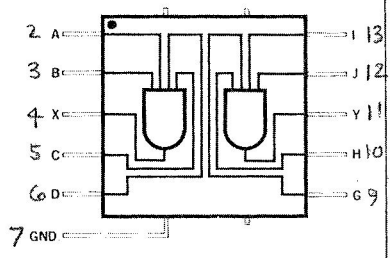


SCHEMATIC DIAGRAM

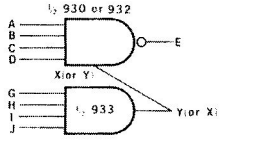


FLAT PACKAGE LAYOUT

(TOP VIEW)



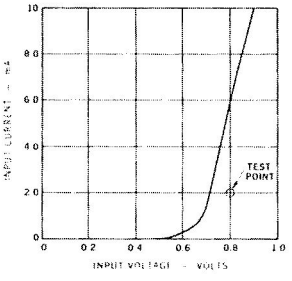
LOGIC EXAMPLE



POSITIVE LOGIC E = A B C D G H I J

NEGATIVE LOGIC E = A + B + C + D + G + H + I + J

FORWARD VOLTAGE VS. FORWARD CURRENT + 25°C

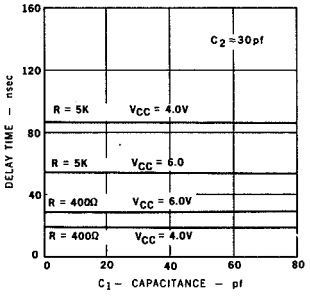


313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA

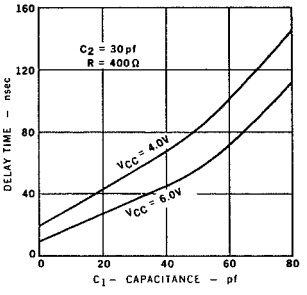
FAIRCHILD SEMICONDUCTOR

Typical Curves to Show the Effects of Extender Pin Capacitance (Resulting From the Use of DTμL 933) on Time Delay of DTμL 930 Dual Gate and DTμL 932 Dual Buffer + 25°C

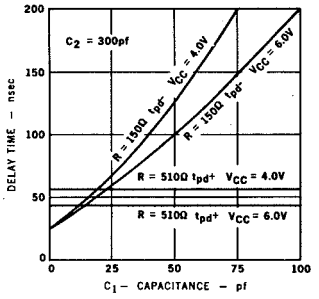
DTμL 930 t_{pd+} VS. EXTENDER PIN CAPACITANCE



DTμL 930 t_{pd-} VS. EXTENDER PIN CAPACITANCE

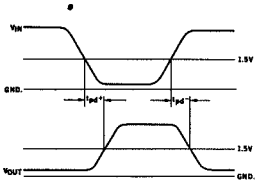


DTμL 932 TIME DELAY VS. EXTENDER PIN CAPACITANCE

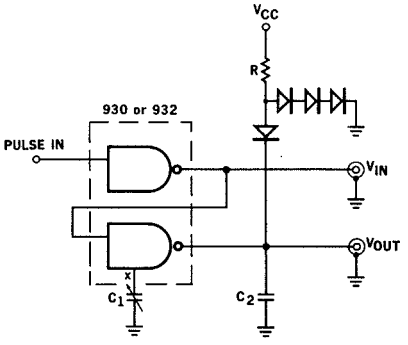


t_{pd-} at R = 5KΩ is slightly lower.

WAVESHAPES



TEST CONDITIONS

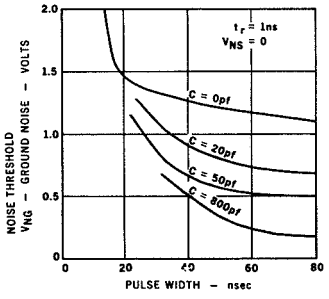


Diodes are FD600

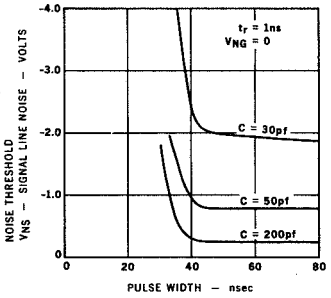
C_1 represents the summation of the DTμL 933Dual Extender Element output capacitances (~5 pf per output) and associated board, connector and wiring capacitances.

Typical Curves to Show the Effects of Extender Pin Capacitance on Noise Threshold of DTμL 930 Dual Gate + 25°C

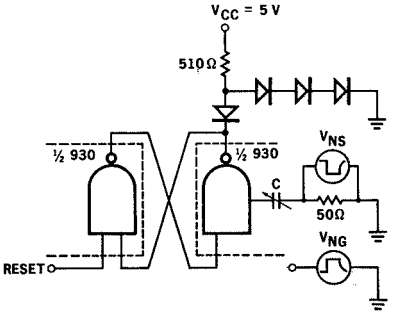
PULSED GROUND NOISE THRESHOLD AS A FUNCTION OF EXTENDER PIN CAPACITANCE



PULSED SIGNAL LINE NOISE THRESHOLD AS A FUNCTION OF EXTENDER PIN CAPACITANCE



TEST CONDITIONS



Diodes are FD600

LPDTμL 9040, 9041 AND 9042
LOW POWER DIODE TRANSISTOR MICROLOGIC™ INTEGRATED CIRCUITS

GENERAL DESCRIPTION

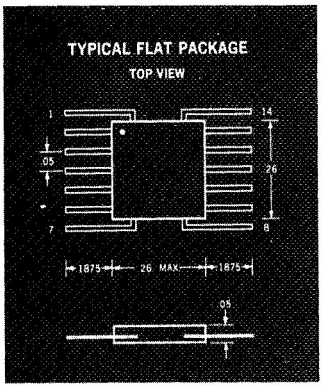
The Fairchild LPDTμL Micrologic™ Integrated Circuit Family consists of a set of compatible, integrated logic circuits specifically designed for low power, medium speed applications.

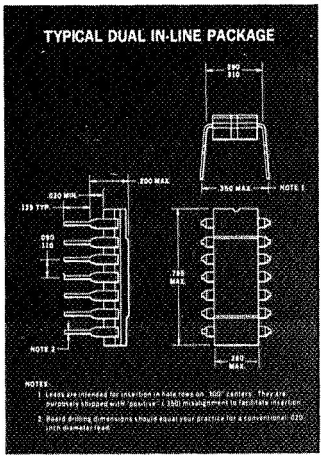
The circuits are fabricated with a silicon monolithic substrate using standard Fairchild Planar epitaxial processes.

Packaging options include the Flat package and the Dual In-Line package.

Important features of the LPDTμL Micrologic™ integrated circuits include the following:

- Reliable operation over the full military temperature range of -55°C to +125°C
- Typical power drains of less than 1 mW per gate (50% duty cycle) for the logic gate elements and less than 4 mW for the clocked flip-flop.
- Single power supply requirement—5 volts optimum, 4.5 to 5.5 volts range.
- Guaranteed fan-out of 10 LPDTμL unit loads or 1 standard Fairchild DTμL unit load, over the full temperature and supply voltage range.
- Guaranteed minimum of 450 mV noise immunity at the temperature extremes.
- Typical logic gate propagation delays of 60 nsec and binary clock rate of 2.5 Mc.
- Emitter follower outputs providing good capacitive drive capability.





ORDER INFORMATION

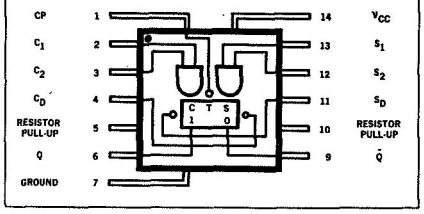
To order Low Power Diode Transistor Micrologic™ integrated circuit elements specify U31XXXX51X for flat package and U6AXXXX51X for Dual In-Line package where XXXX is 9040, 9041 or 9042.

LPDTμL 9040 CLOCKED FLIP-FLOP

DESCRIPTION

The LPDTμL 9040 element is a directly coupled, dual-rank flip-flop suitable for use in counters, shift registers and other storage applications. Either R-S or J-K mode operation is possible. Direct set and clear inputs are provided which override all other data inputs.

LOGIC DIAGRAM SHOWING FLAT OR DUAL-IN LINE PACKAGE PIN ASSIGNMENT



SYNCHRONOUS ENTRY TRUTH TABLES

R-S MODE OPERATION

INPUTS @t_n				OUTPUTS @t_{n+1}	
S_1	S_2	C_1	C_2	Q	$\overline{Q}$
13	12	2	3	6	9
L	X	L	X	NC	NC
L	X	X	L	NC	NC
X	L	L	X	NC	NC
X	L	X	L	NC	NC
L	X	H	H	L	H
X	L	H	H	L	H
H	H	L	X	H	L
H	H	X	L	H	L
H	H	H	H	AMBIGUOUS	

J-K MODE OPERATION

INPUTS @t_n		OUTPUTS @t_{n+1}	
S_1	C_1	Q	$\overline{Q}$
13	2	6	9
L	L	NC	NC
L	H	L	H
H	L	H	L
H	H	TOGGLES	

ASYCHRONOUS ENTRY TRUTH TABLE

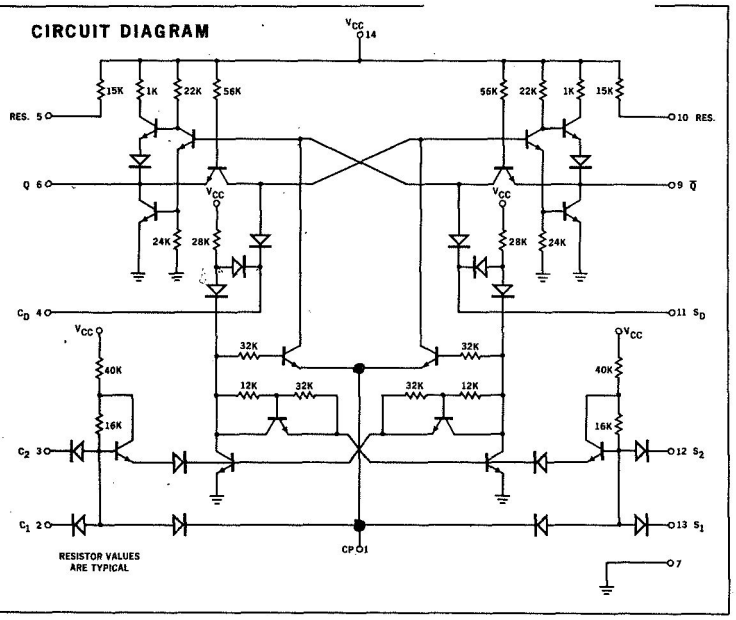
INPUTS		OUTPUTS	
S_D	C_D	Q	$\overline{Q}$
11	4	6	9
H	H	NC	NC
H	L	L	H
L	H	H	L
L	L	H	H

Symbols

H - Most positive logic level
L - Most negative logic level
X - Either H or L can be present
NC - No change in state

NOTES:
1. For J-K mode operation connect Pin 6 to Pin 3 and Pin 9 to Pin 12.
2. Asynchronous entries override all synchronous entries.

CIRCUIT DIAGRAM



LOADING RULES

INPUT	*NORMALIZED UNIT LOADS (U.L.)
$\frac{S_1\ S_2}{C_1\ C_2}$	0.75 U.L.
$S_D\ C_D$	2.5 U.L.
CP	2.5 U.L.
OUTPUT	**FAN-OUT**
Q, $\overline{Q}$	10 U.L. 7 U.L. WITH RESISTOR PULL-UP CONNECTED

*1UNIT LOAD EQUALS 1-LPDTμL 9041 OR 9042 INPUT LOAD

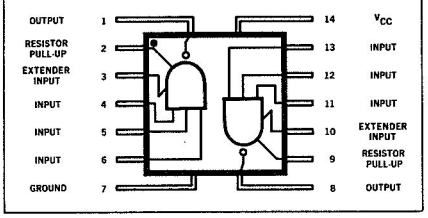
LPDTμL 9042 — DUAL 3 INPUT NAND GATE WITH EXTENDER INPUTS

DESCRIPTION

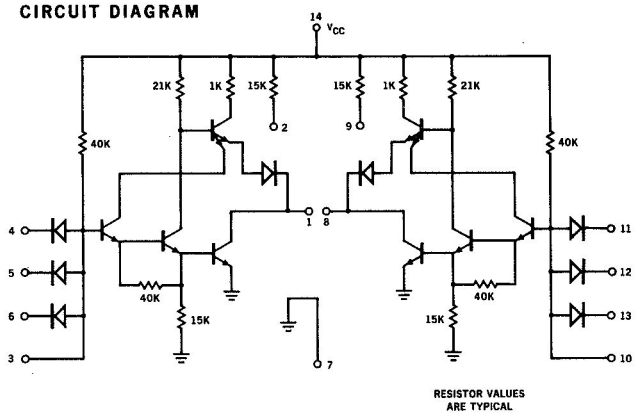
The LPDTμL 9042 element consists of two 3-input positive logic NAND gates with extender inputs. This element in the family allows the user to implement logic applications requiring a gate fan-in exceeding three.

The DTμL 9933 4-input extender element or equivalent—may be used to provide additional diode inputs. Any capacitance added to the extender input will increase the turn-on delay of the LPDTμL 9042 gate. Typically, the increase is 10 ns/pico-farad. Turn-off delay is not affected.

LOGIC DIAGRAM SHOWING FLAT OR DUAL-IN-LINE PACKAGE PIN ASSIGNMENT

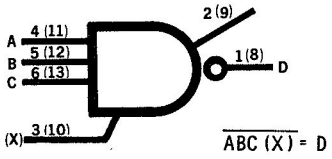


CIRCUIT DIAGRAM



RESISTOR VALUES ARE TYPICAL

POSITIVE LOGIC NAND GATE



$\overline{ABC}$ (X) = D

EACH INPUT = 1 UNIT LOAD

OUTPUT FAN-OUT = 10 UNIT LOADS

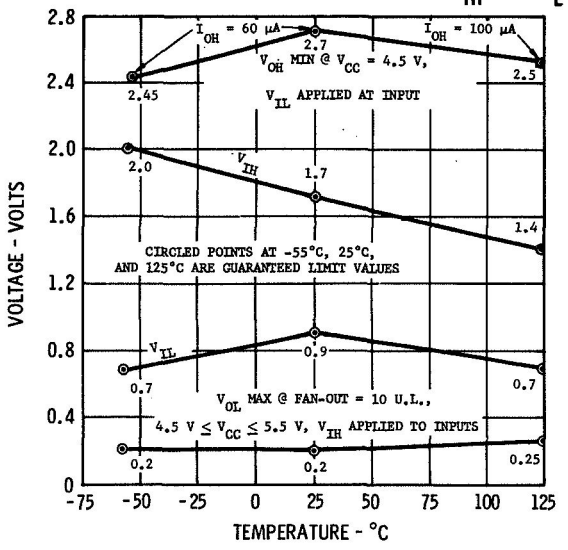
= 7 UNIT LOADS WITH RESISTOR PULL-UP CONNECTED

BUFFER ELEMENT

For applications requiring a fan-out exceeding ten, the Fairchild DTμL 9930 Dual 4-Input Gate may be used. The DTμL 9930 will drive 24 LPDTμL unit loads, while maintaining the same output logic levels as the low power circuits.

The input of a DTμL 9930 requires the equivalent of 10 LPDTμL unit loads. Therefore, a low power circuit can drive only one DTμL 9930 input.

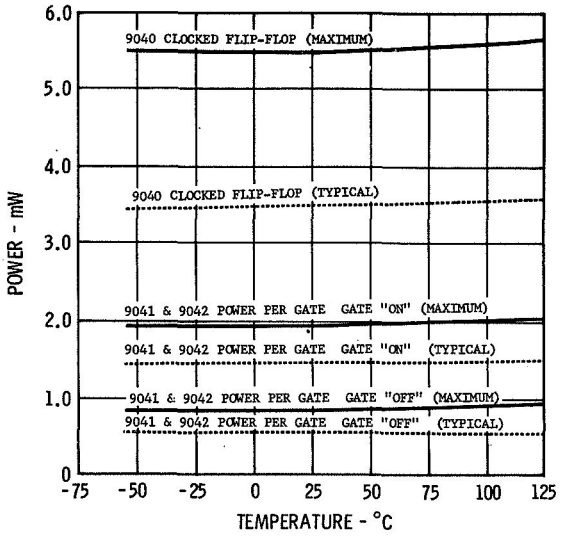
OPERATING VOLTAGE CHARACTERISTICS



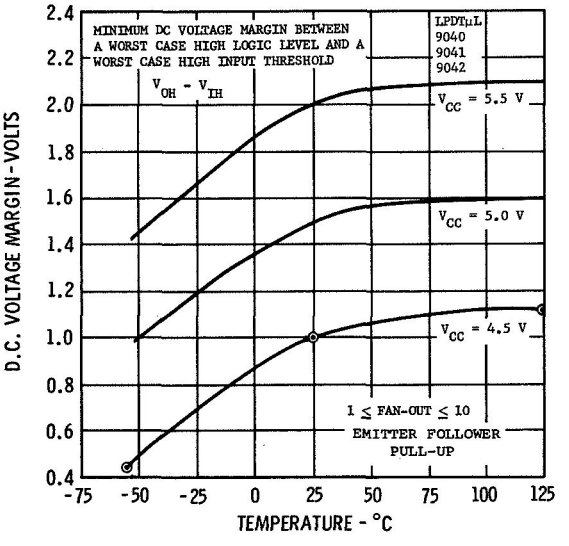
POWER CHARACTERISTICS

VCC = 5V

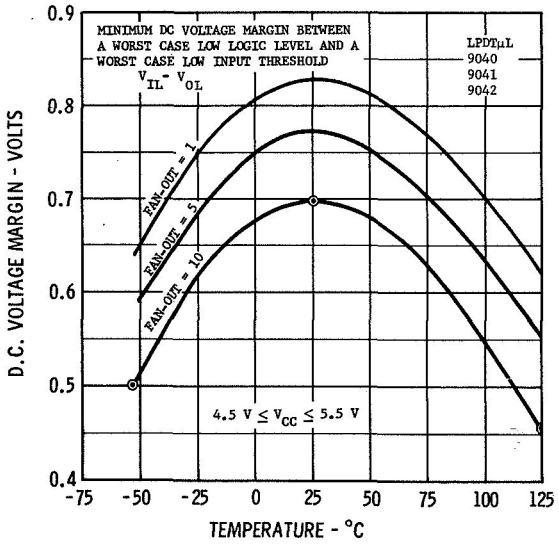
EMITTER FOLLOWER PULL-UP



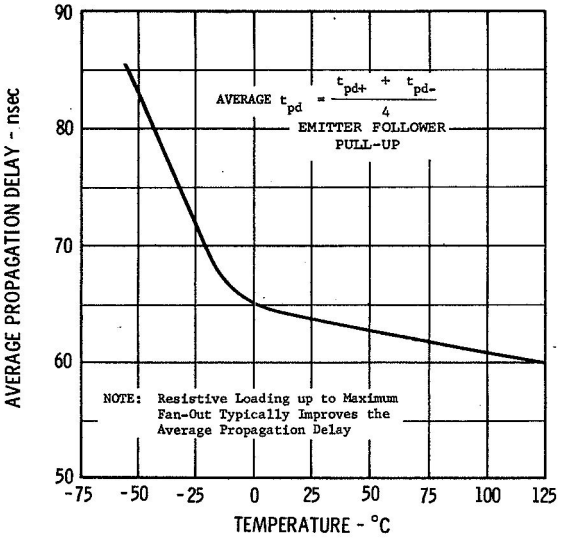
HIGH LEVEL NOISE IMMUNITY



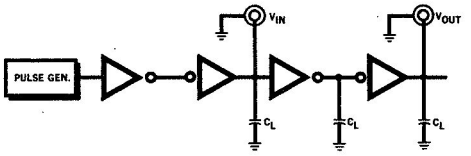
LOW LEVEL NOISE IMMUNITY



TYPICAL AVERAGE PROPAGATION DELAY LPDTμL 9041 • 9042



TEST CIRCUIT

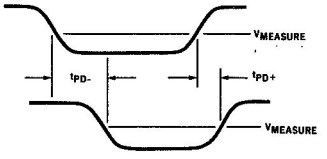


CONDITIONS

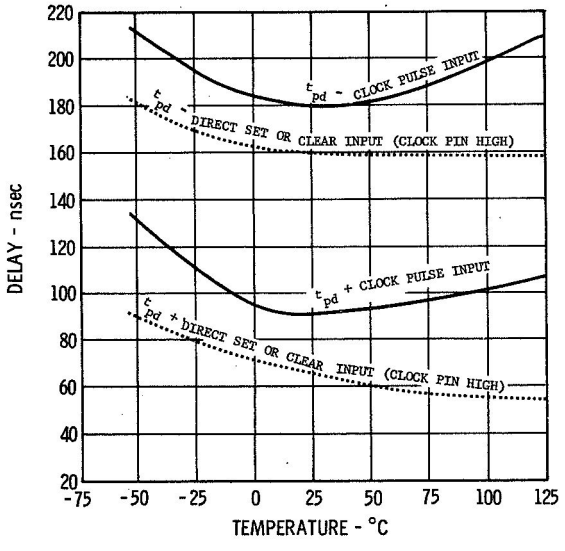
V_{CC} = 5.0V, C_L = 50pf (INCLUDING PROBE AND JIG CAPACITANCE)

$V_{MEASURE}$ = 1.6V @ -55°C
(GND. REF.) 1.3V @ 25°C
0.9V @ 125°C

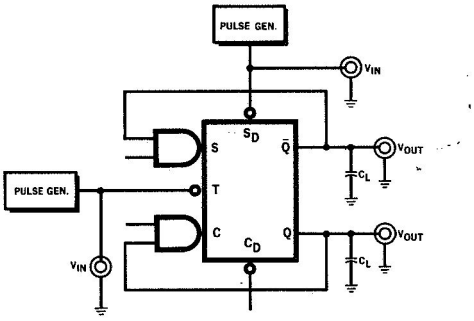
WAVE FORMS



TYPICAL DELAY CHARACTERISTICS LPDTμL 9040



TEST CIRCUIT



CONDITIONS

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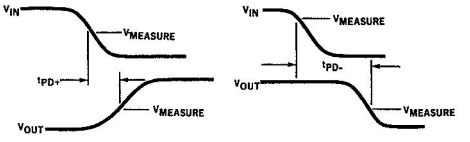
$V_{MEASURE}$ = 1.6V @ -55°C
(GND. REF.) 1.3V @ 25°C
0.9V @ 125°C

WAVE FORMS



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